

# SENSORES DE IMAGEM CMOS

José Gabriel Rodríguez Carneiro Gomes

EPOLI/DEL e COPPE/PEE

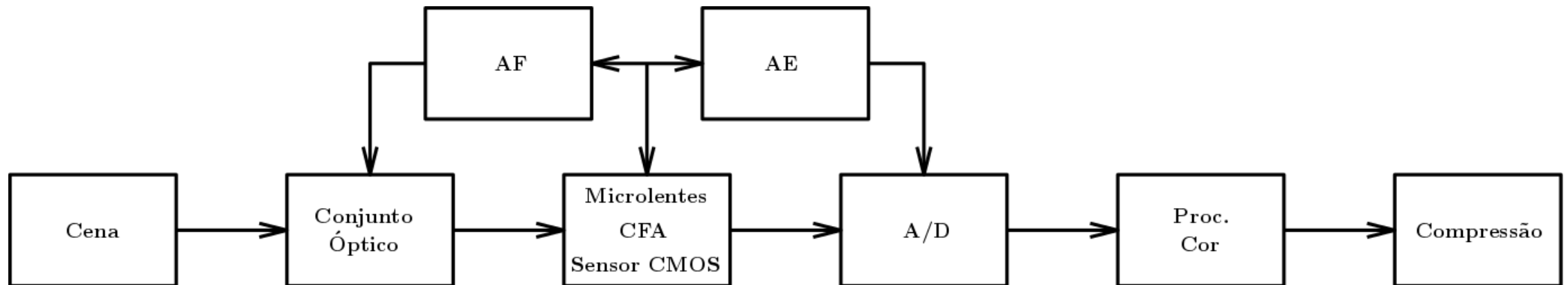
Universidade Federal do Rio de Janeiro

# CONTEÚDO

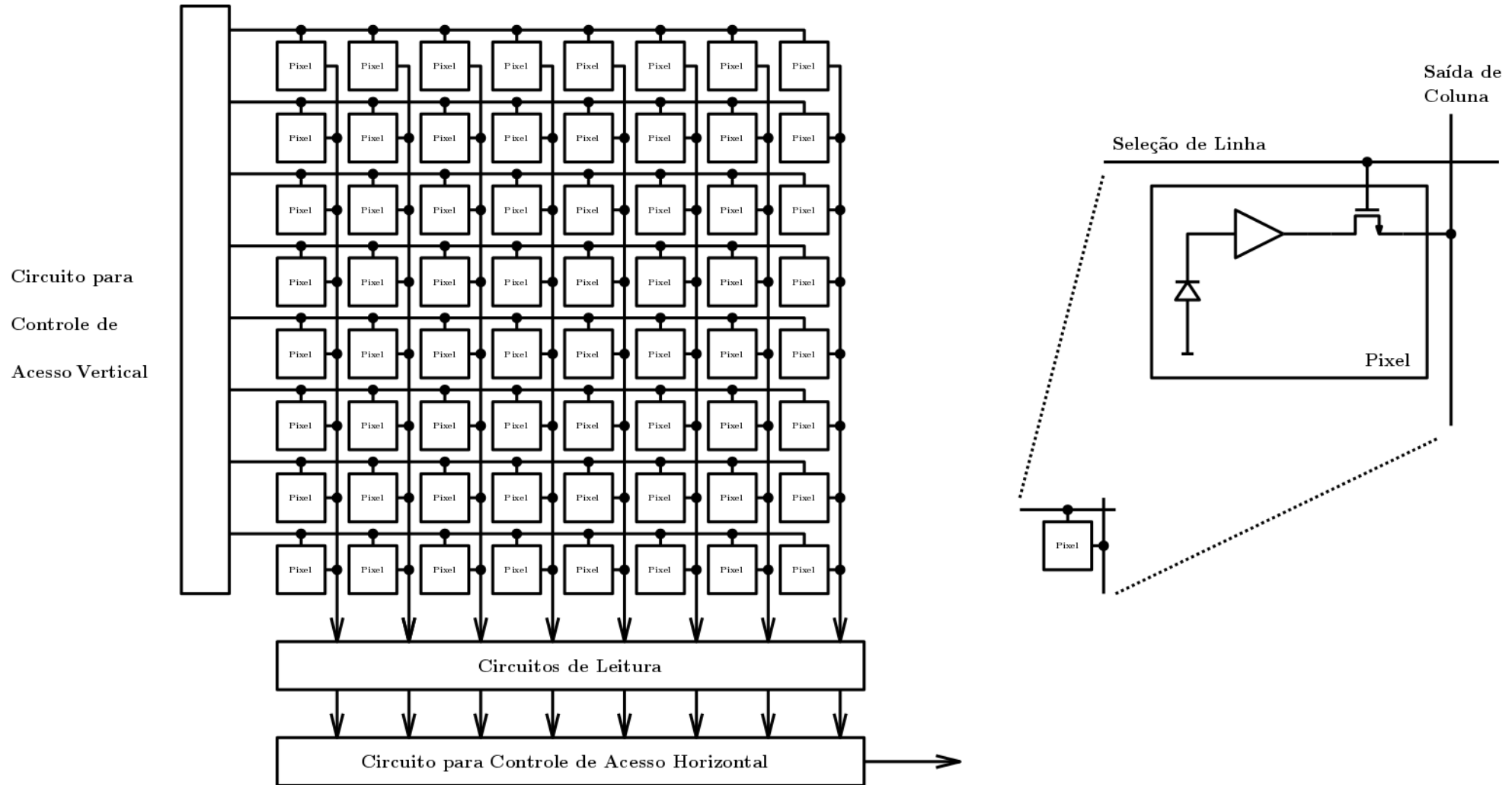
- **Sensor de Imagem CMOS**
- **Pixel**
- **Processamento de Imagens no Plano Focal**
- **Conclusões e Referências**

# SENSOR DE IMAGENS CMOS

- Diagrama de blocos de um sistema eletrônico básico de imagem



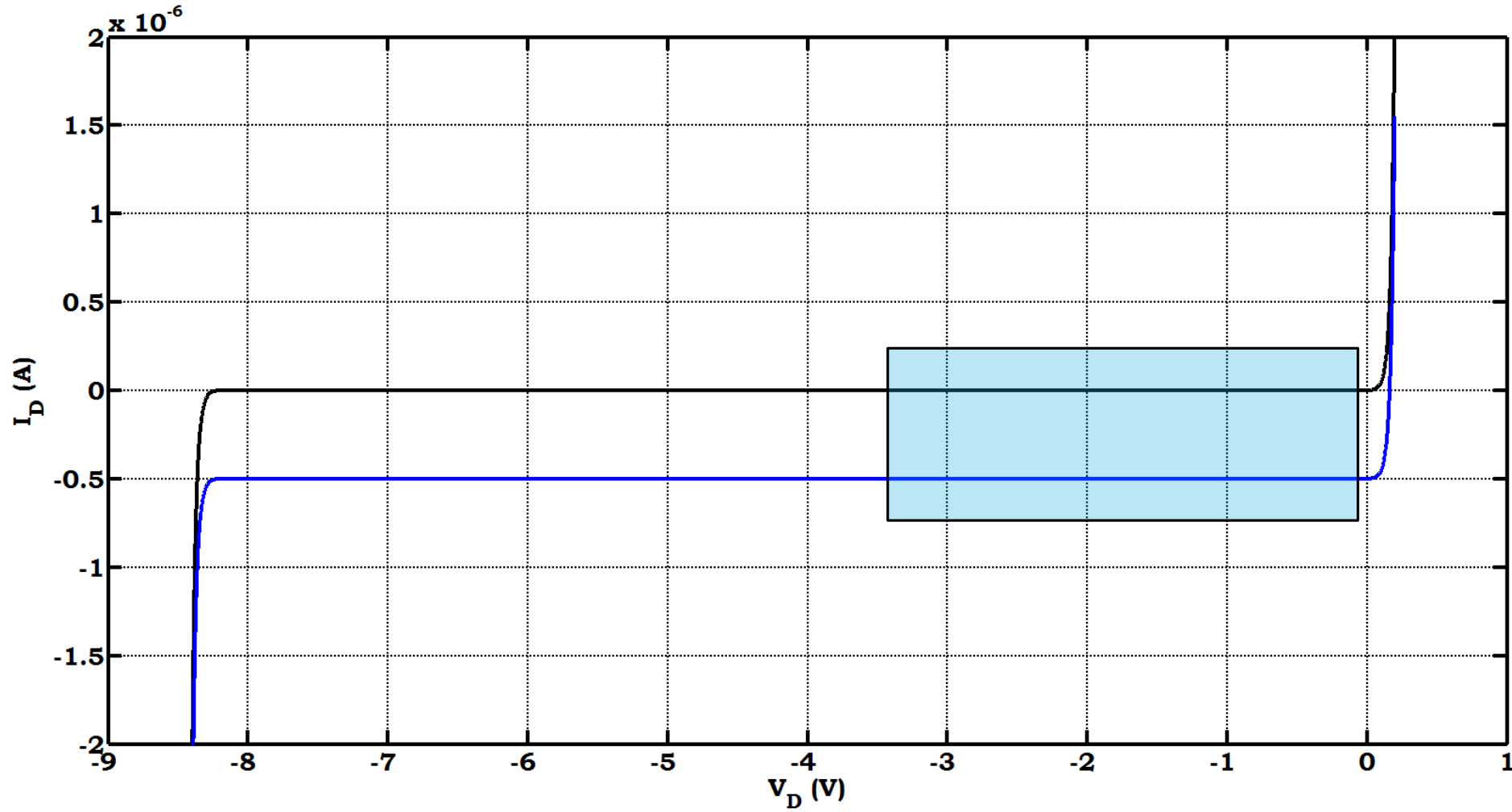
# SENSOR DE IMAGENS CMOS



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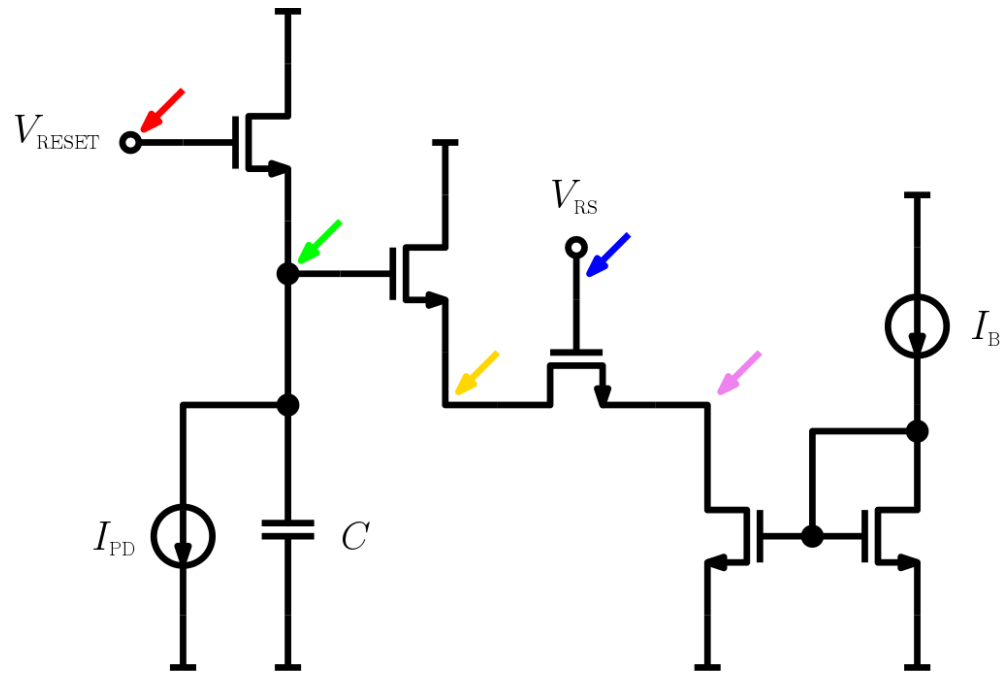
- **Passive-pixel sensor (1960)**
- **Charge-coupled devices (1970) – Willard S. Boyle e George E. Smith, Prêmio Nobel 2009**
- **Active-pixel sensor (final dos anos 80) – 3T, logarítmico**
- **4T (anos 90)**
- **Processamento de imagens no plano focal (meados dos anos 90, anos 2000)**

# FOTODIODO

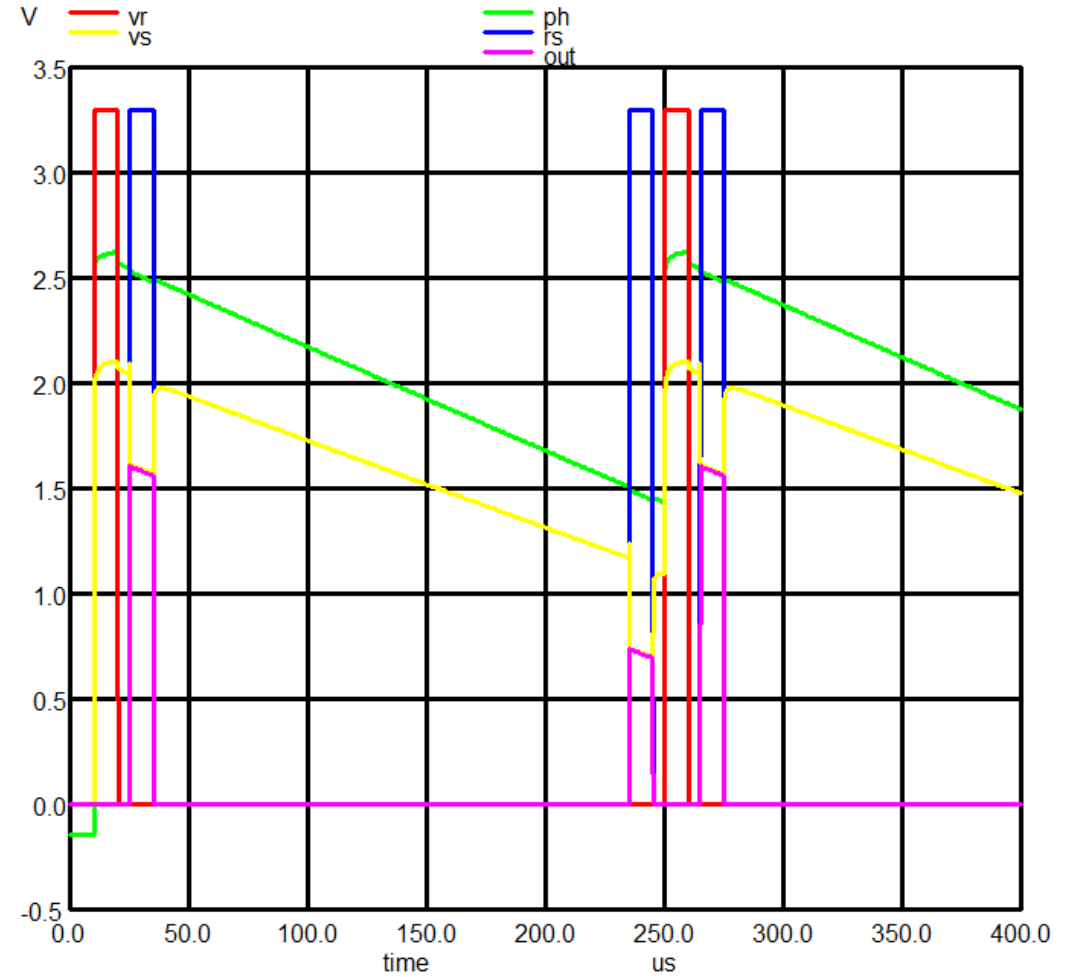


```
pts=5000; a=-8.4; b=0.2; stp=(b-a)/pts; x=a:stp:(b-stp); y=zeros(size(x));  
h=find(x>=0); y(h)=(1e-9)*(exp(x(h)/0.026)-1);  
i=find(x<0); y(i)=-(1e-9)*(exp((abs(x(i))-8.2)/0.026)-1);  
plot(x,y,'k','LineWidth',3); hold on; grid on;  
plot(x,y-5e-7,'b-','LineWidth',3); axis([-9 1 -2e-6 2e-6]);  
xlabel('V_{D} (V)'); ylabel('I_{D} (A)');
```

# PIXEL 3T

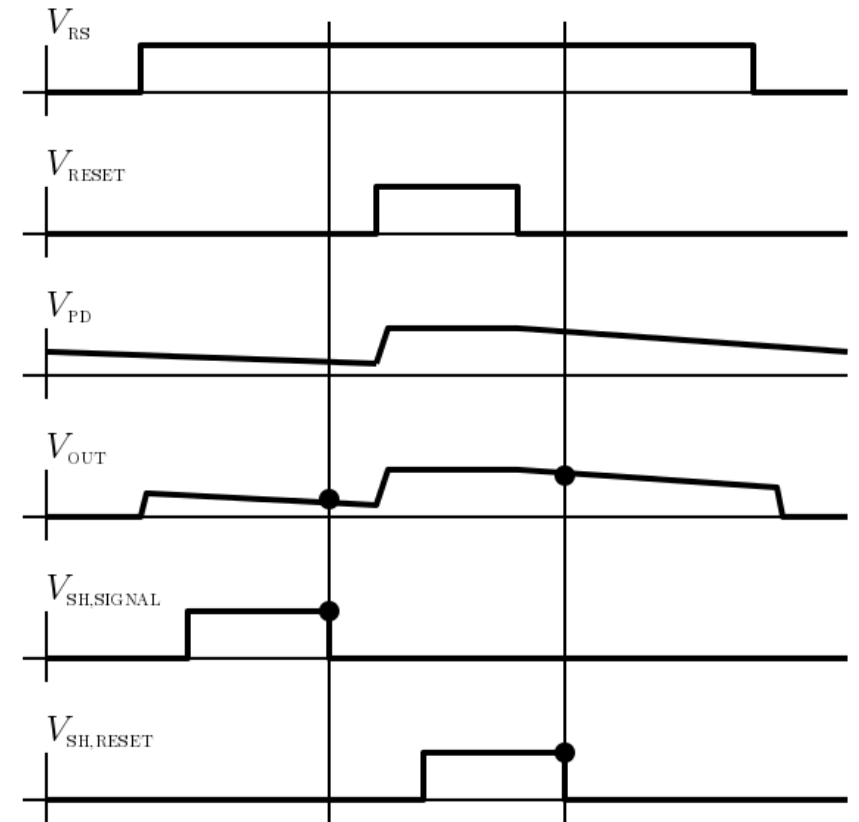
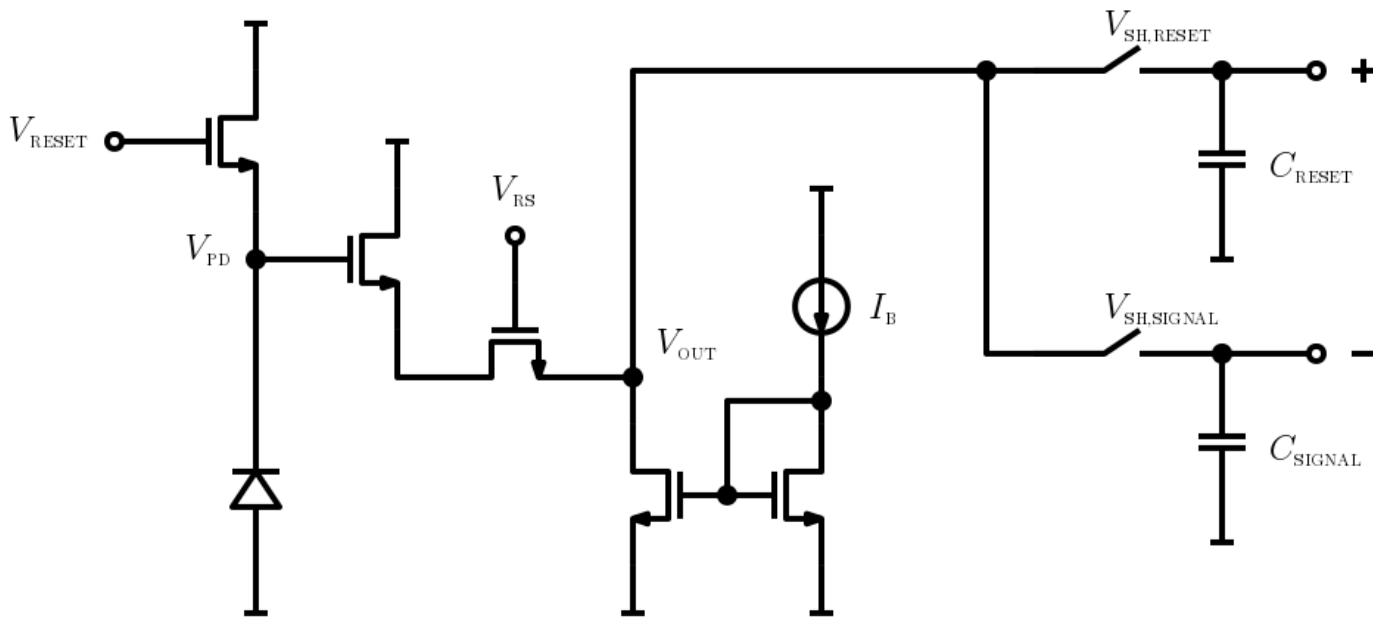


Tecnologia  $0.35 \mu\text{m}$ ,  $C = 10 \text{ fF}$ ,  $I_{\text{ph}} = 50 \text{ pA}$ ,  $I_{\text{B}} = 2 \mu\text{A}$



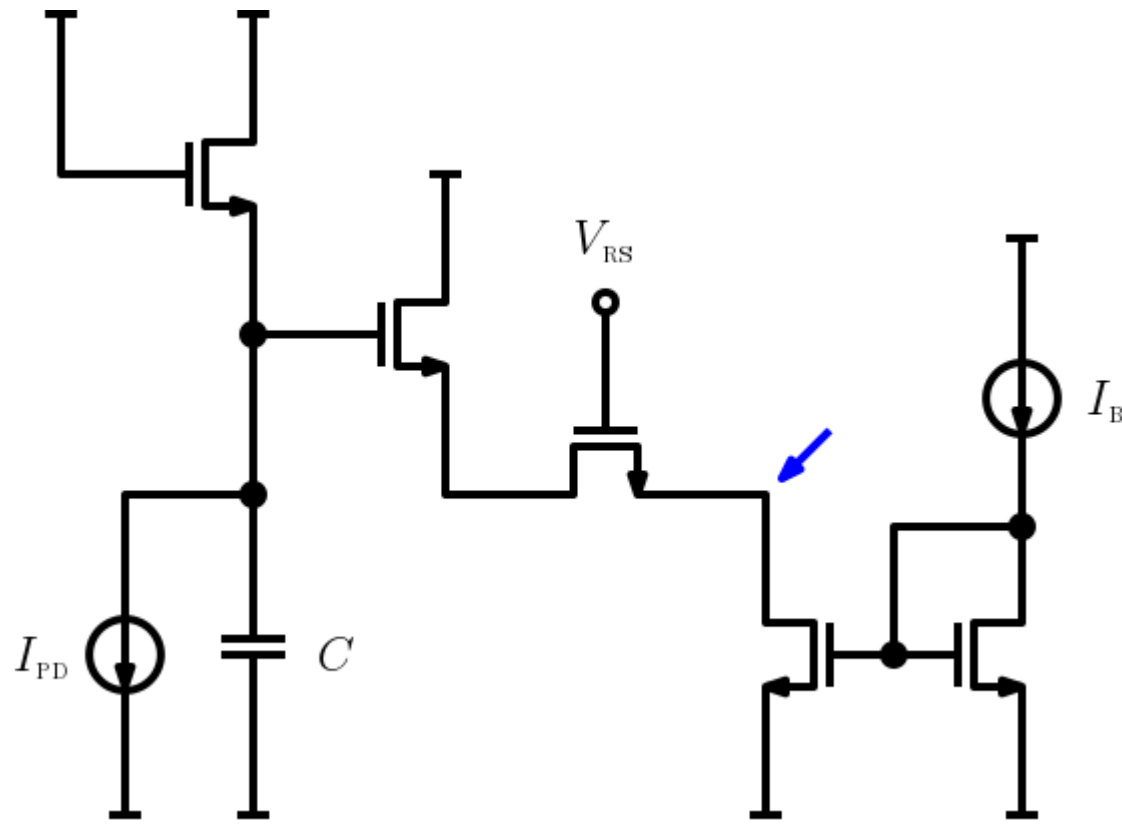
# 3T E AMOSTRAGEM DUPLA CORRELACIONADA

- Conhecida pela sigla CDS (Correlated Double-Sampling)





# PIXEL LOGARÍTMICO



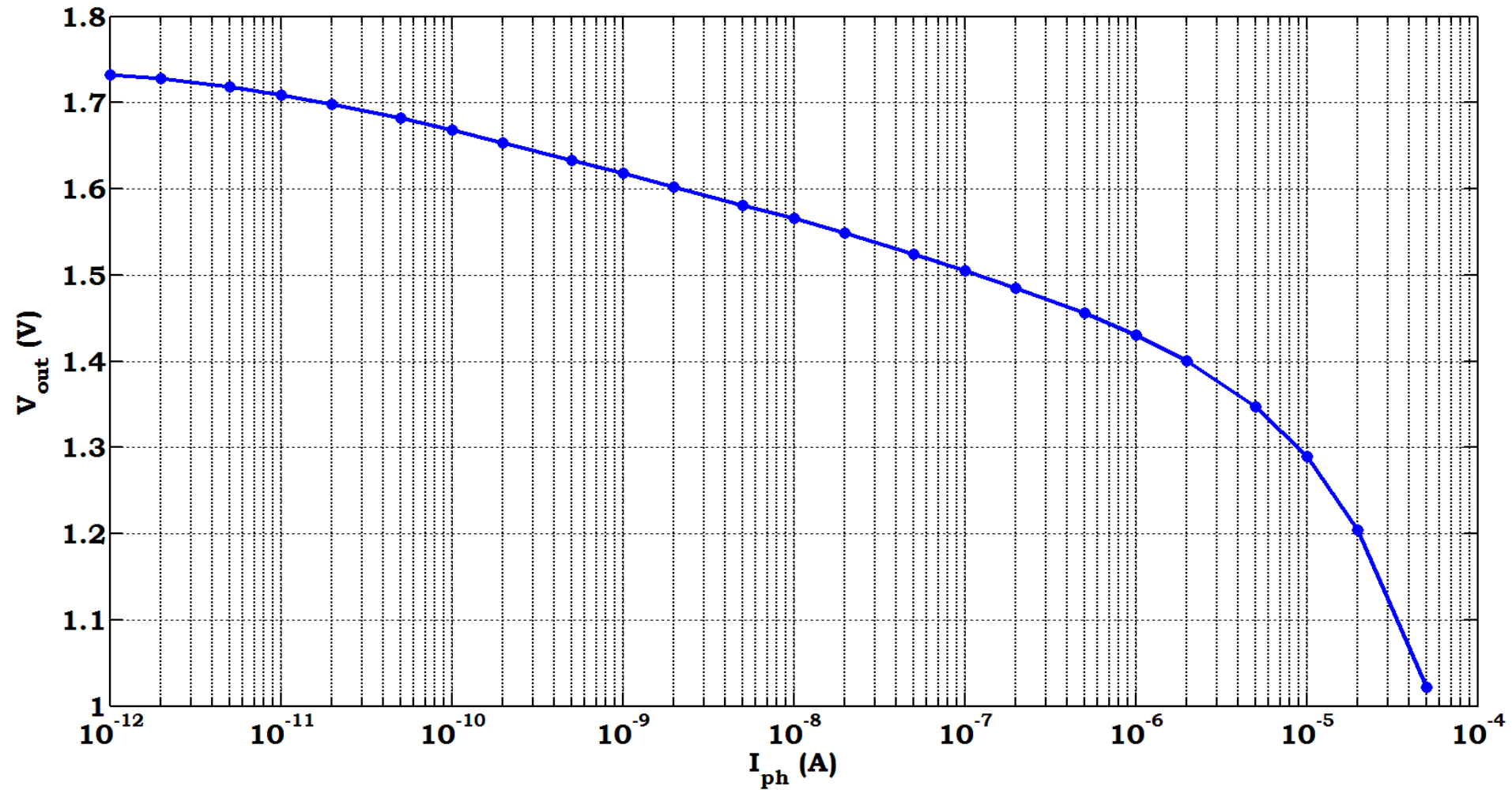
Operação em modo “sub-threshold”:

$$I_D \approx 1 \text{ nA}$$

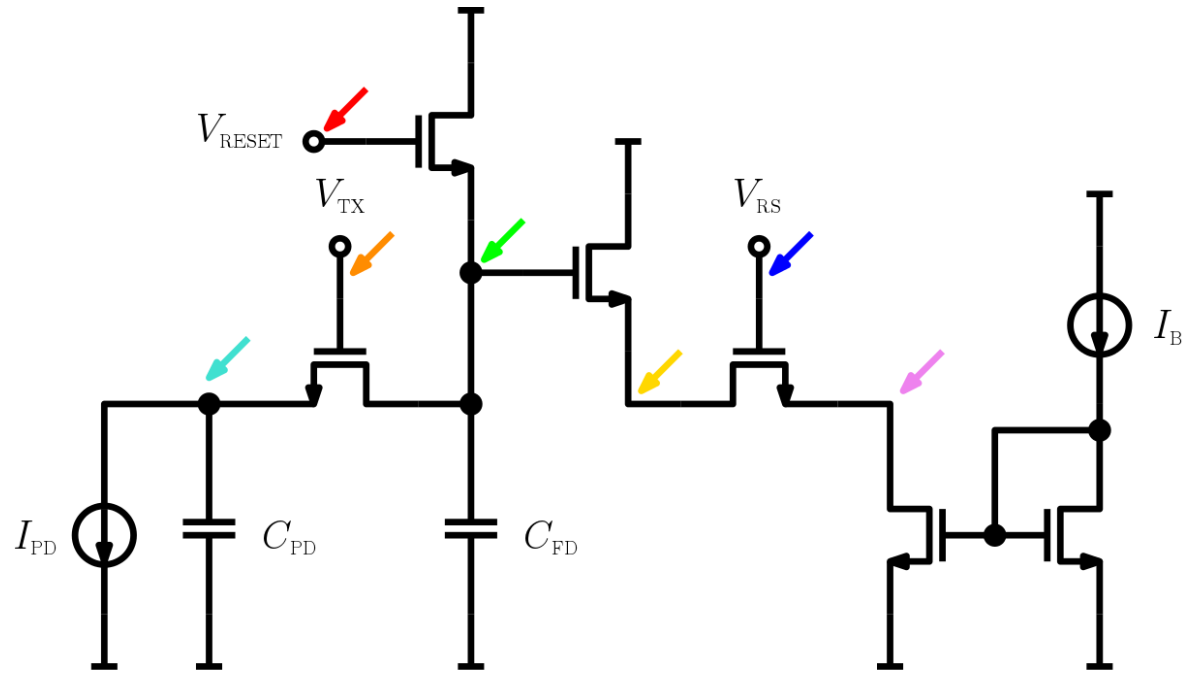
$$I_D = \alpha \exp((V_{DD} - V_{PD})/\beta)$$

$$V_{PD} = V_{DD} - \beta \ln(I_D/\alpha)$$

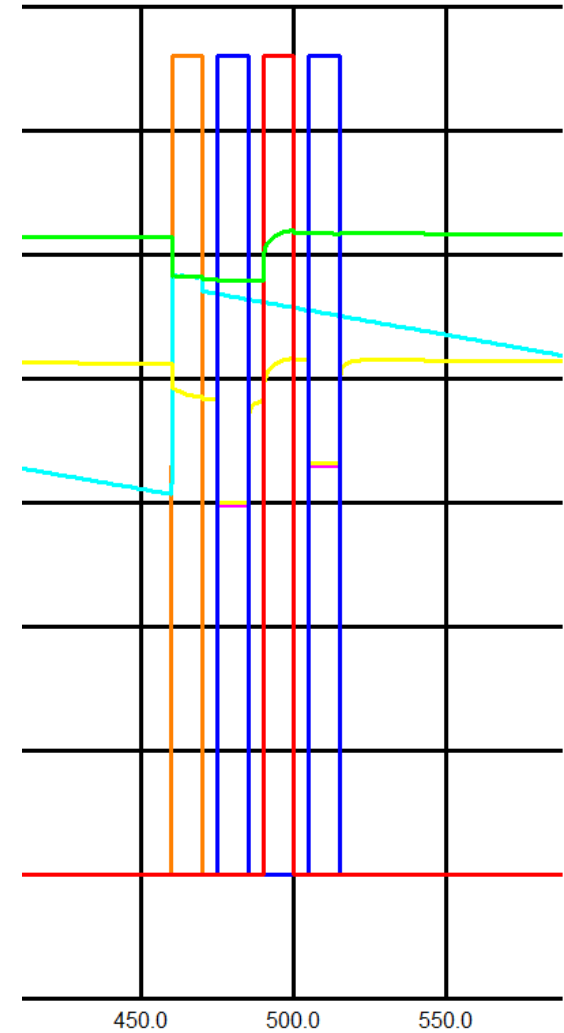
# PIXEL LOGARÍTMICO



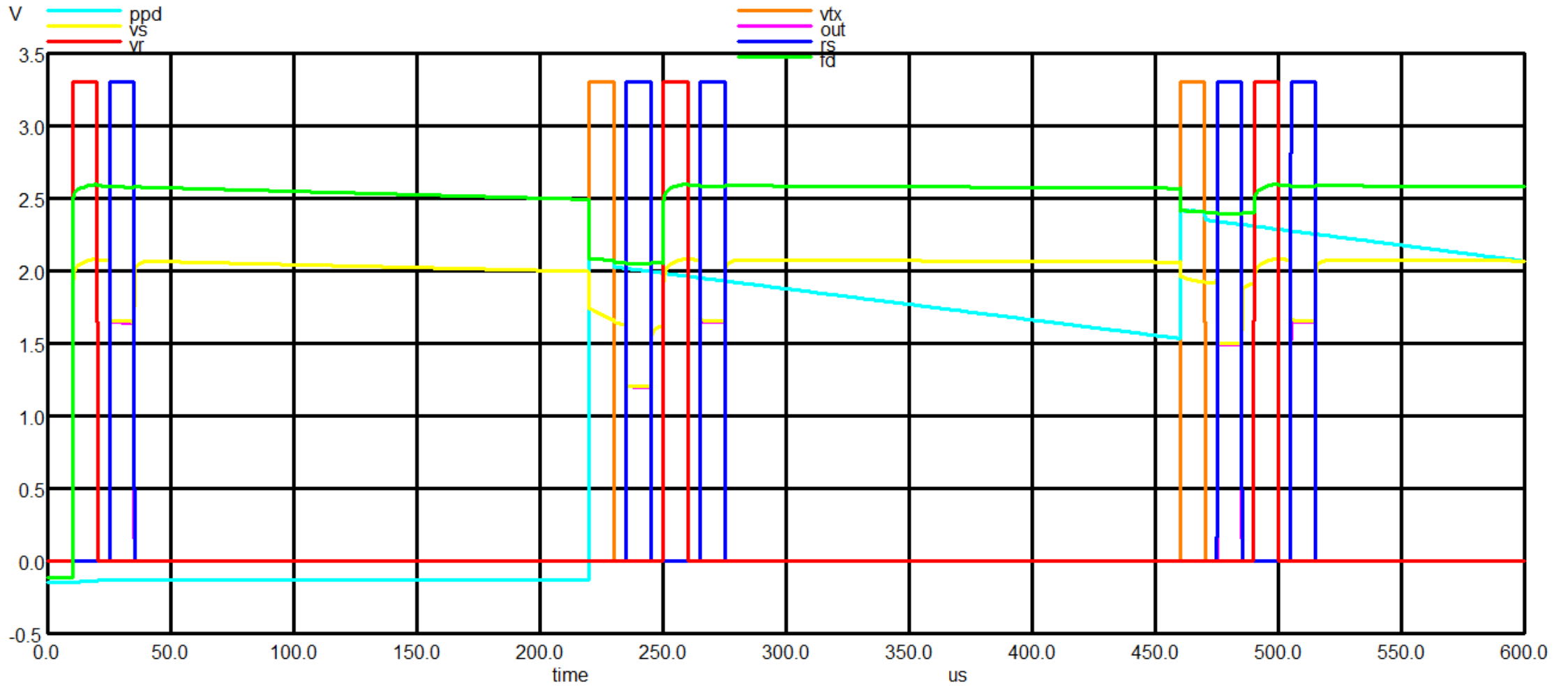
# PIXEL "4T" SEM PPD



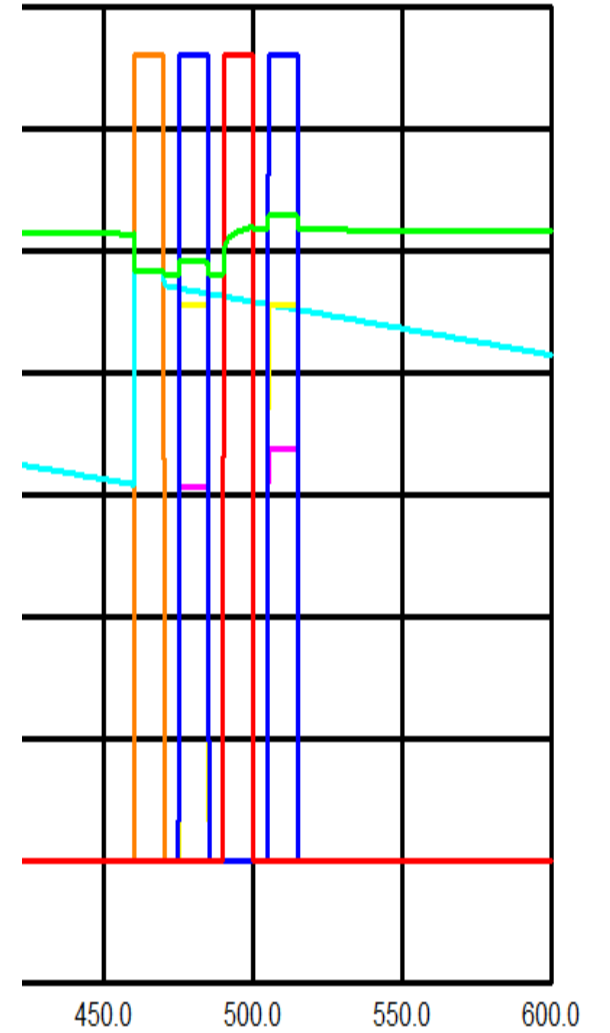
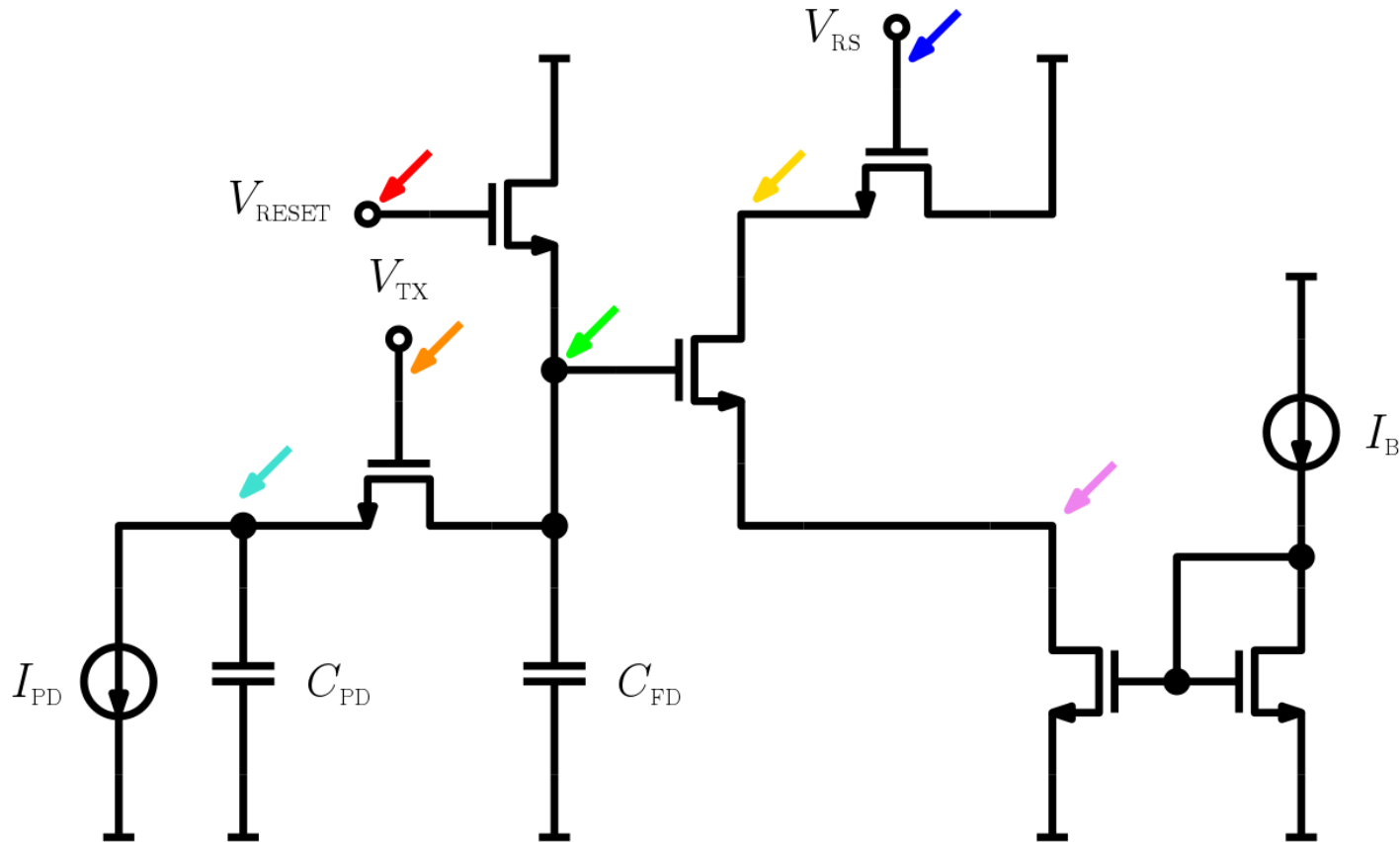
Tecnologia 0.35  $\mu\text{m}$ ,  $C_{PD} = 10 \text{ fF}$ ,  $I_{ph} = 20 \text{ pA}$ ,  $C_{FD} = 50 \text{ fF}$ ,  $I_B = 2 \text{ }\mu\text{A}$



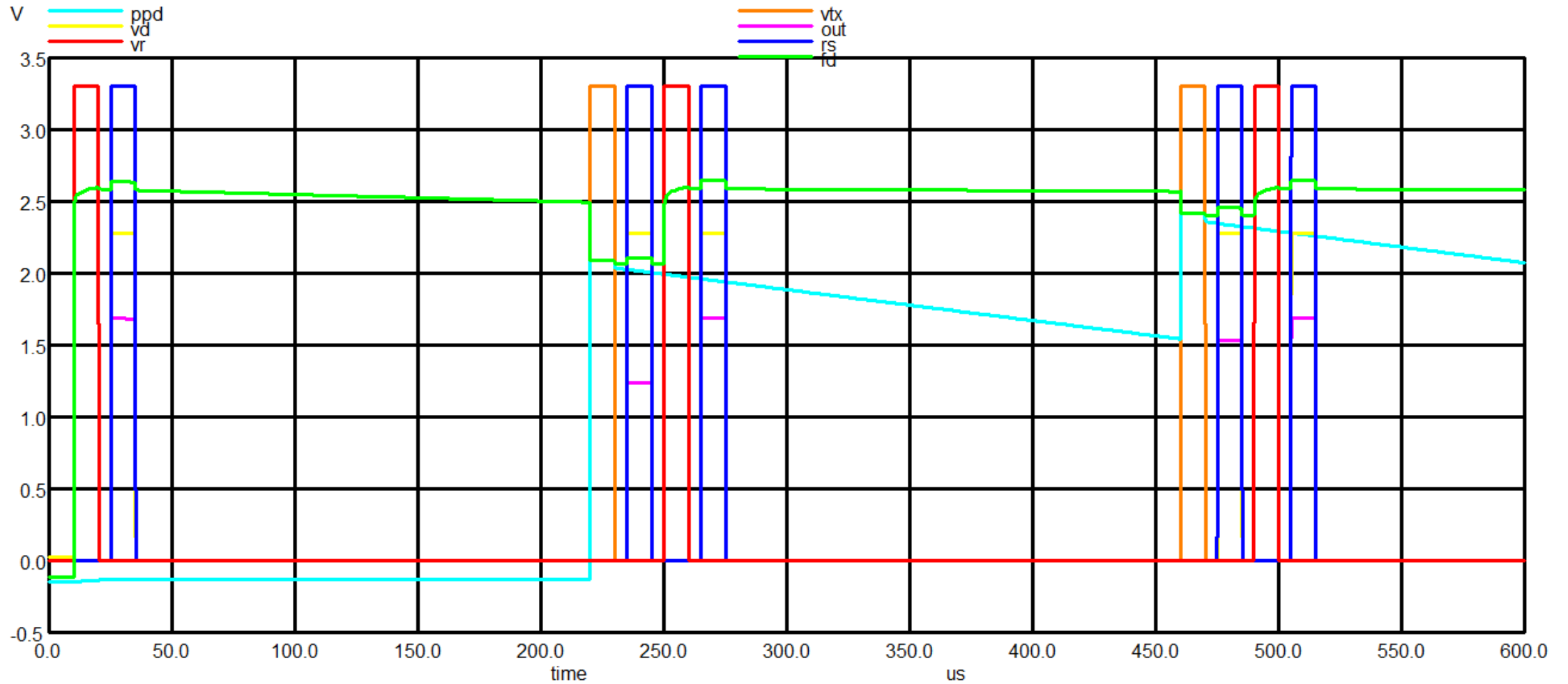
# PIXEL "4T" SEM PPD



# BOOSTING (TAMBÉM PARA PIXEL 3T)

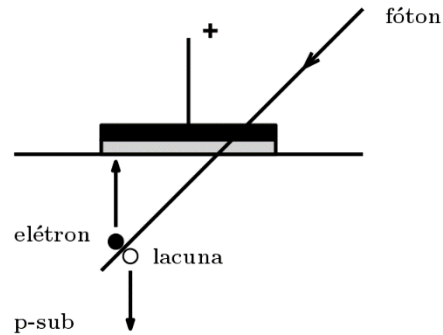


# BOOSTING (TAMBÉM PARA PIXEL 3T)

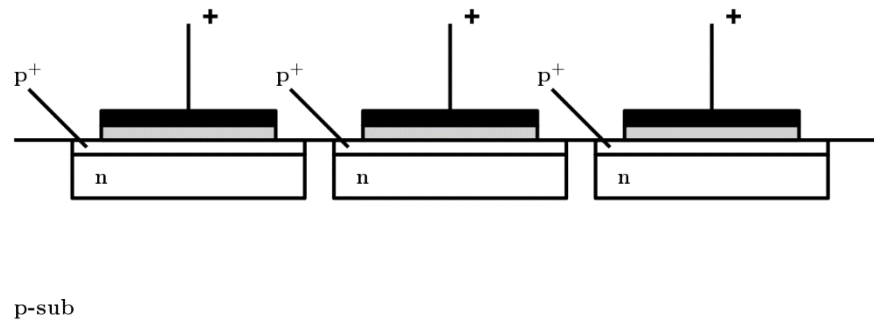


# CHARGE-COUPLED DEVICE (CCD)

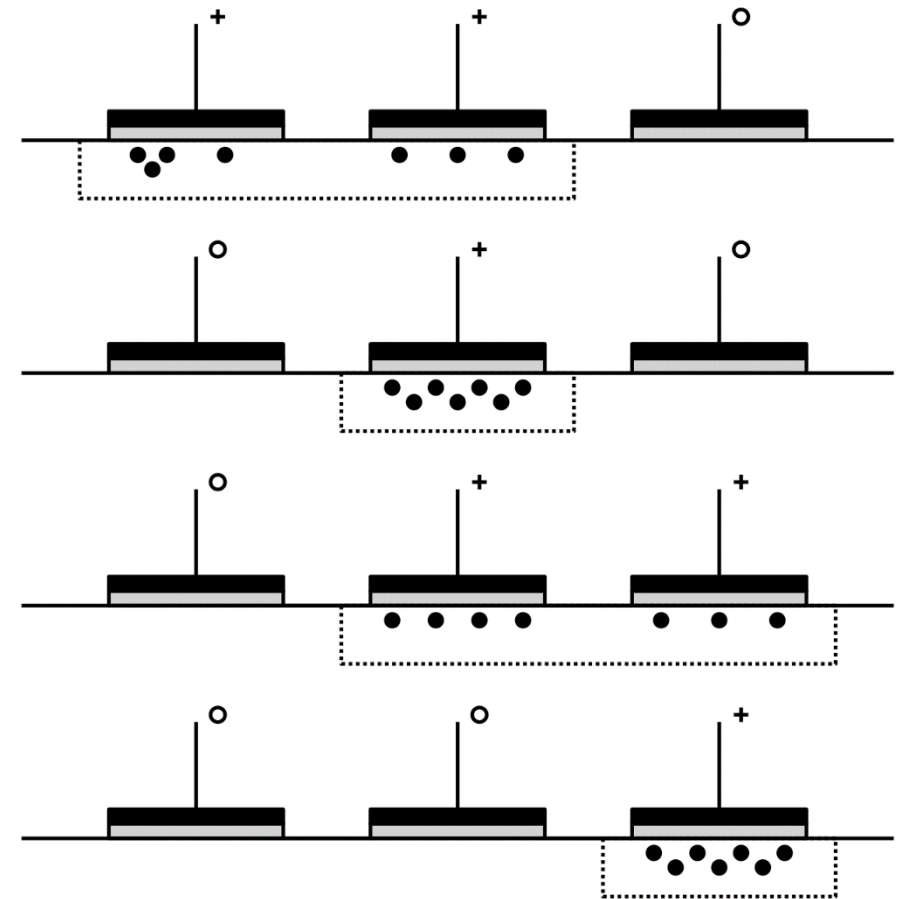
Capacitor MIS (metal-insulator-silicon):



Implante p<sup>+</sup> aumenta enormemente a eficiência da transferência de carga:

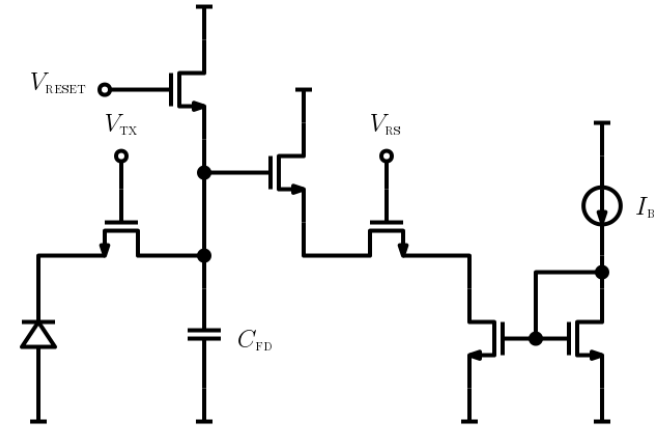
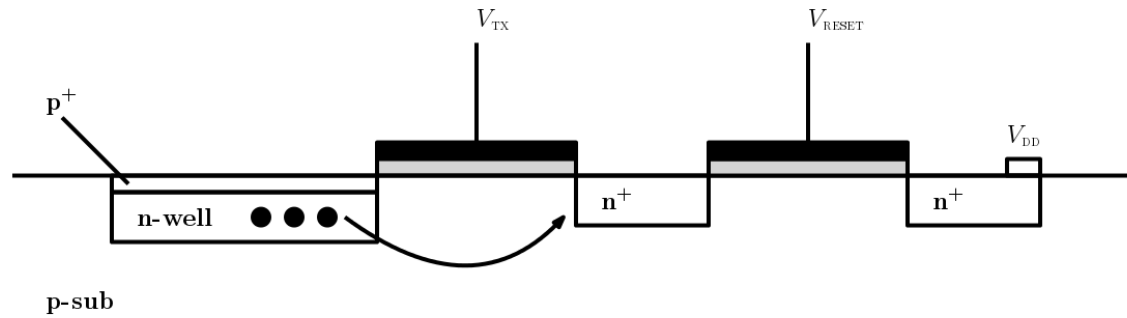


Transferência de carga (CCD de três fases):

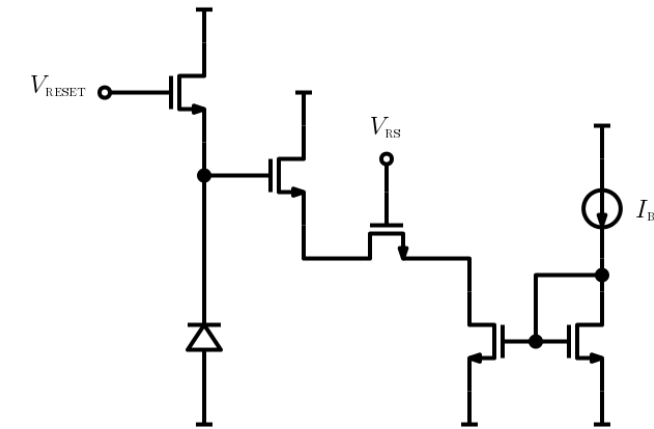
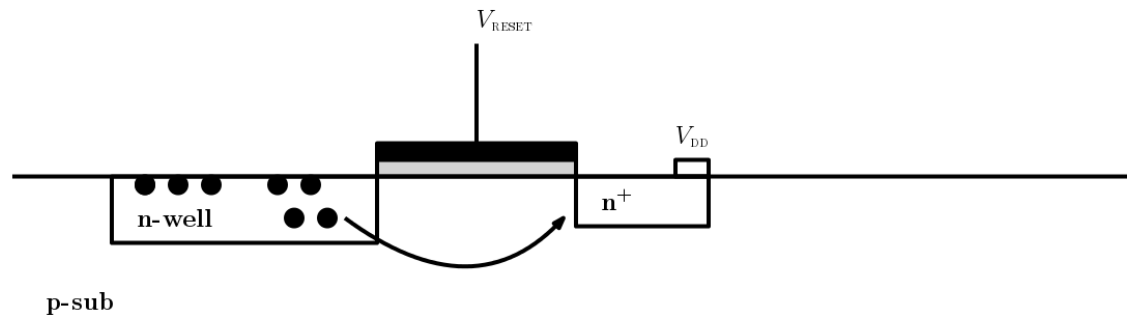


# PIXEL 4T – PINNED PHOTODIODE (PPD)

No PPD, a transferência de carga é completa (todo o poço é esvaziado):

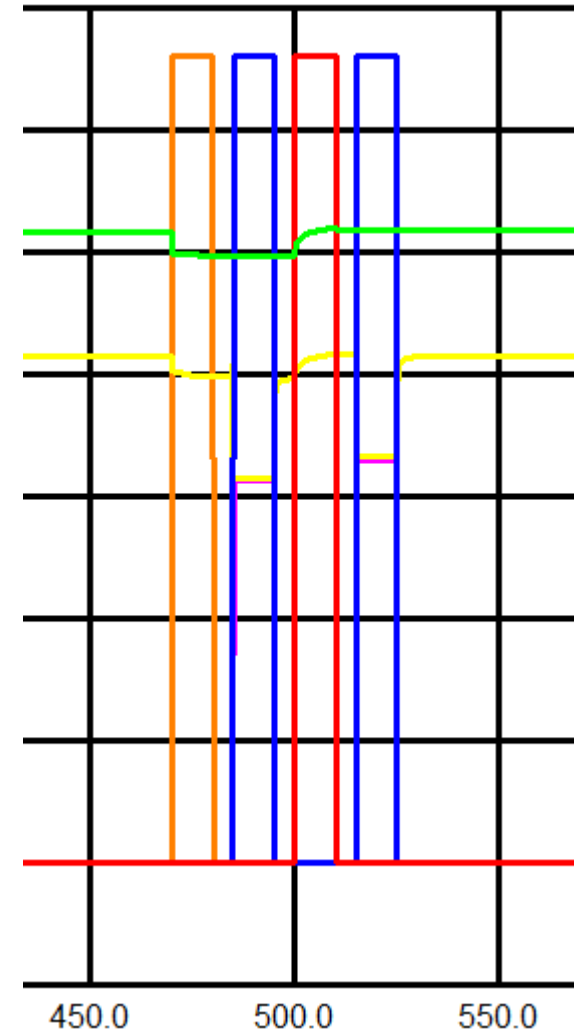
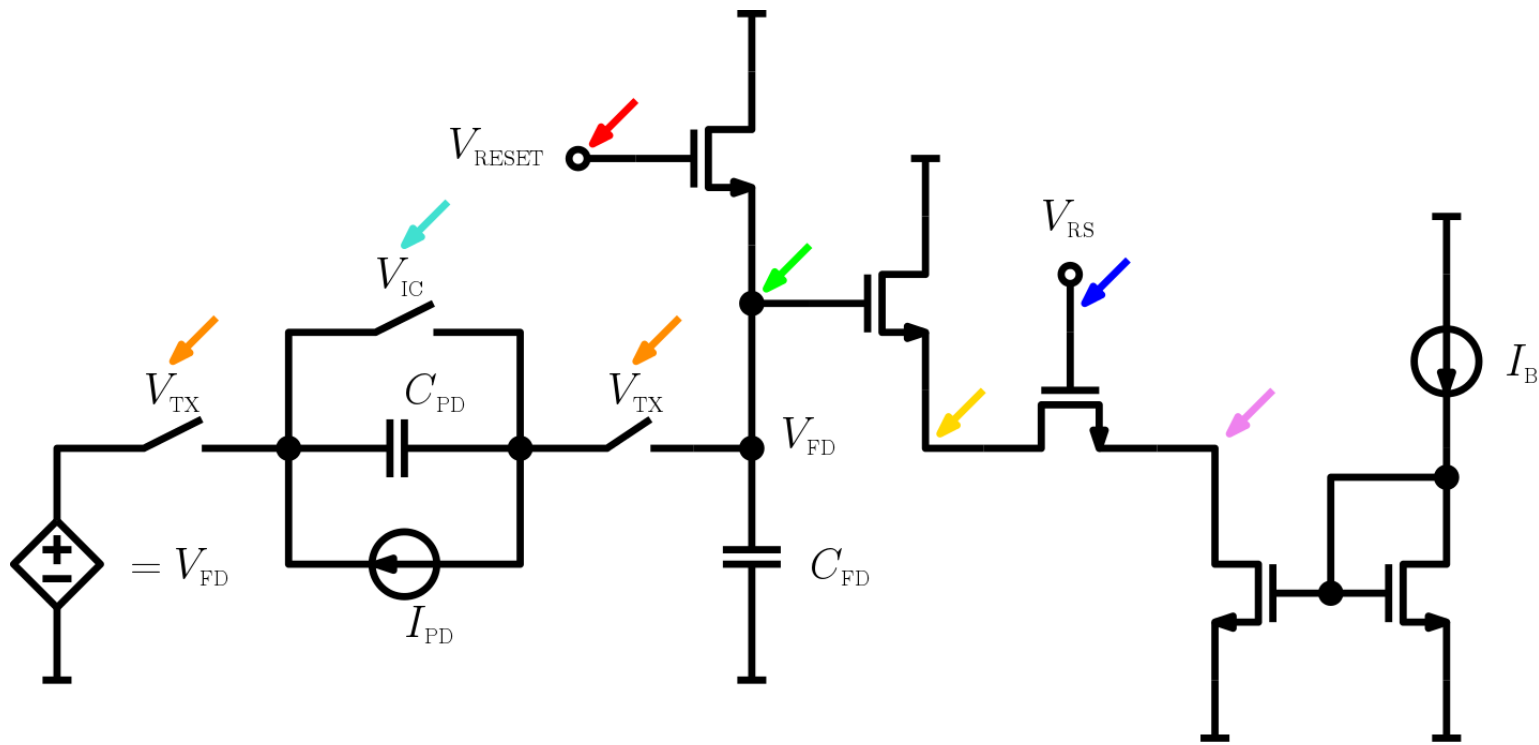


No fotodiodo comum (n-well/p-sub), ocorre perda de portadoras de carga devido a estados de interface:

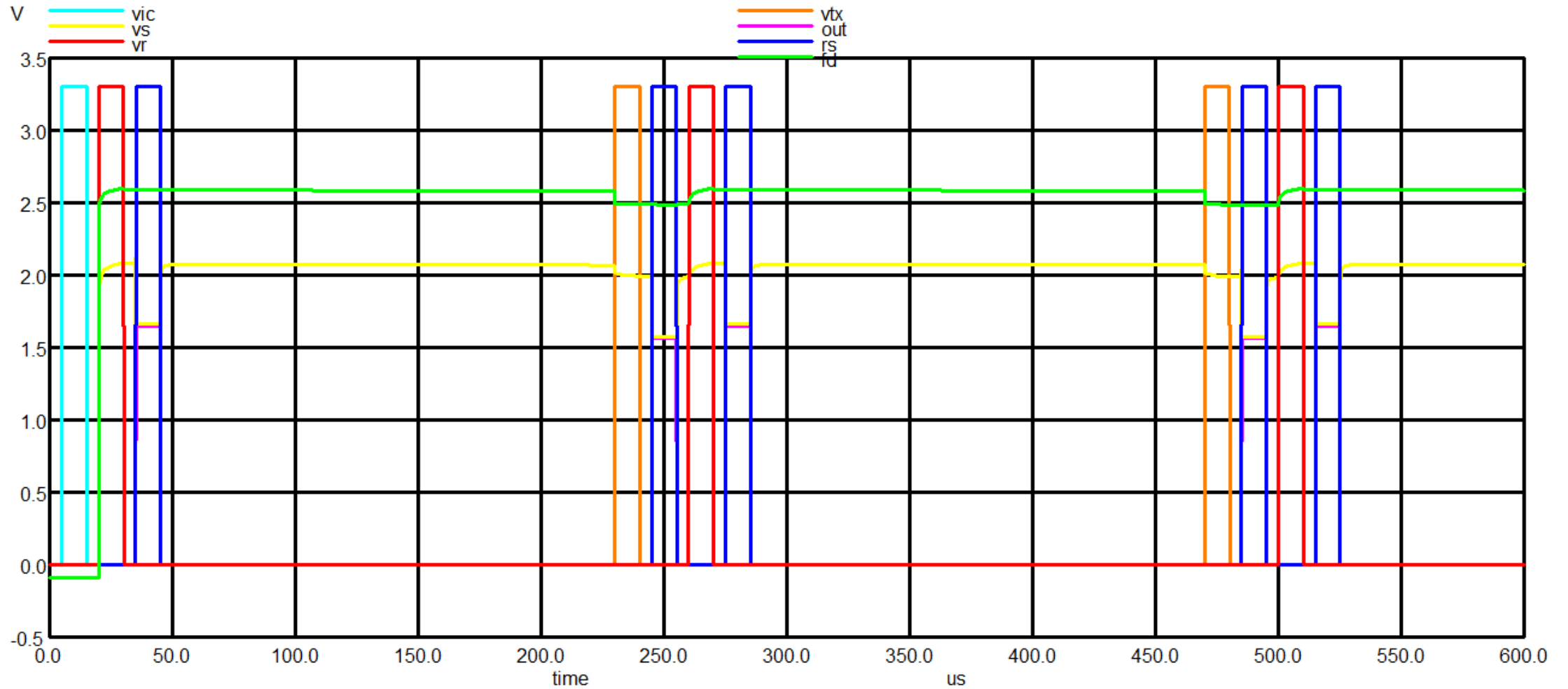




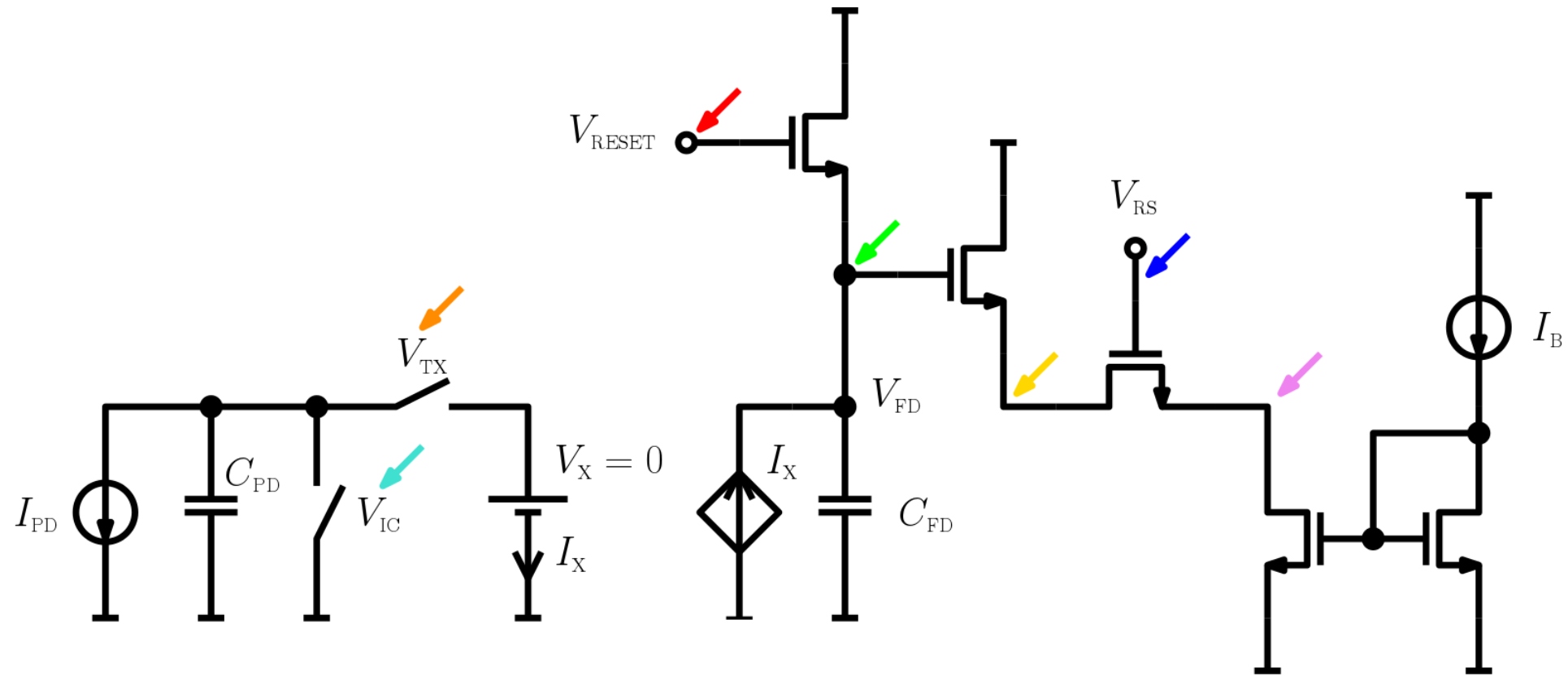
# PIXEL 4T – PINNED PHOTODIODE (PPD)



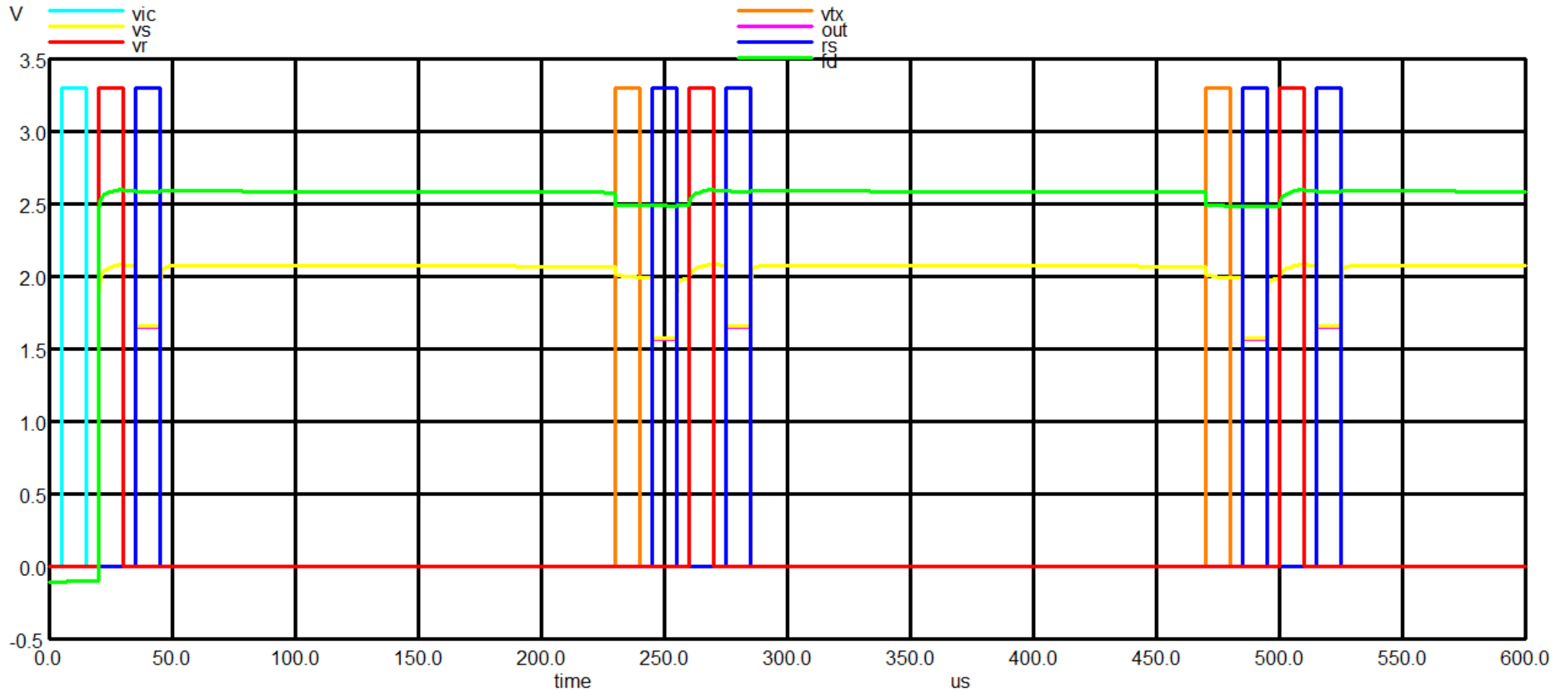
# PIXEL 4T – PINNED PHOTODIODE (PPD)



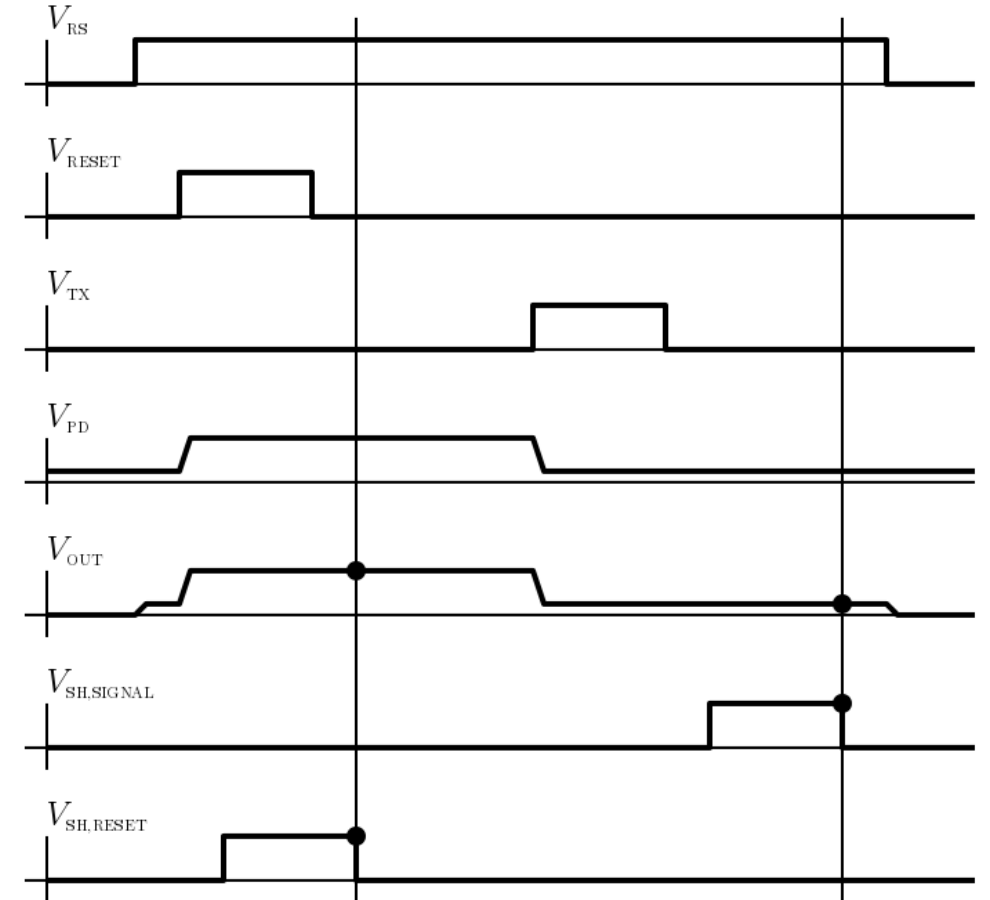
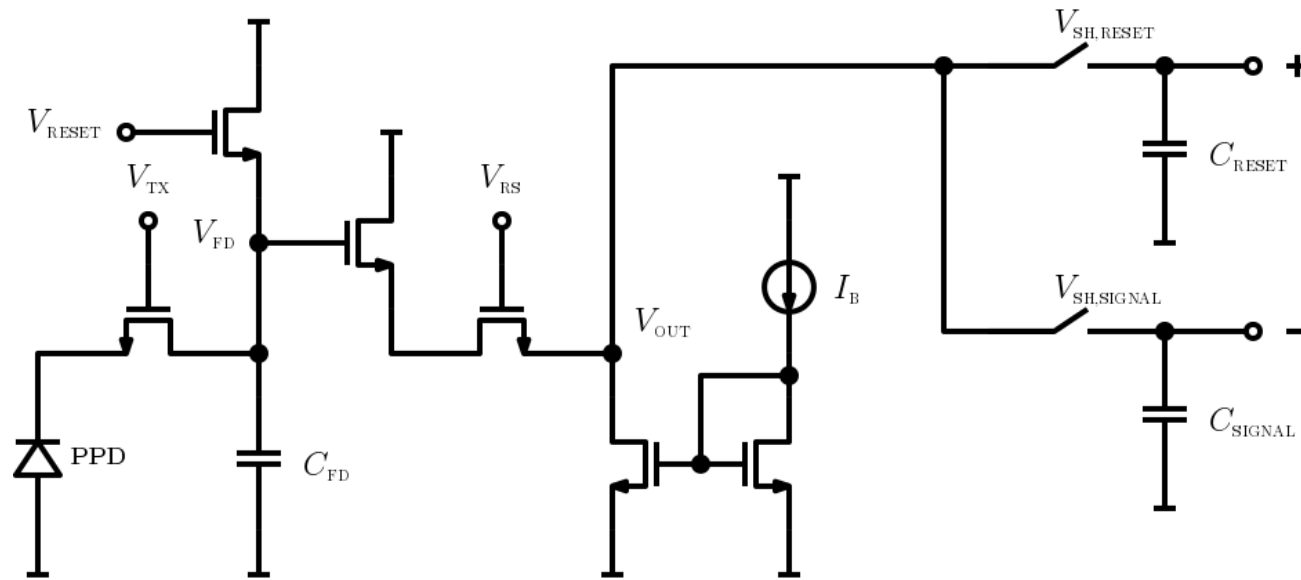
# PIXEL 4T – PINNED PHOTODIODE (PPD)



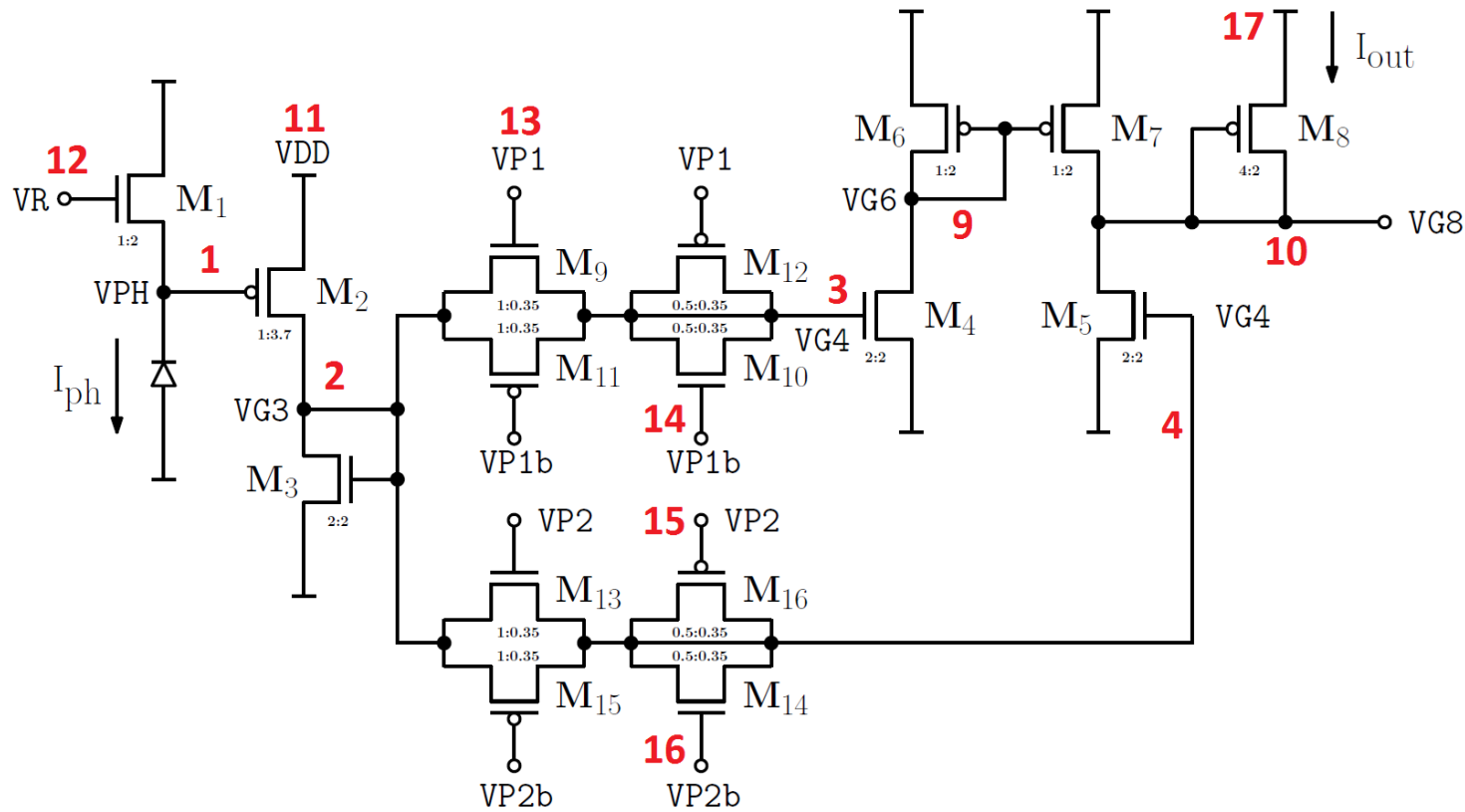
# PIXEL 4T – PINNED PHOTODIODE (PPD)



# 4T E AMOSTRAGEM DUPLA CORRELACIONADA

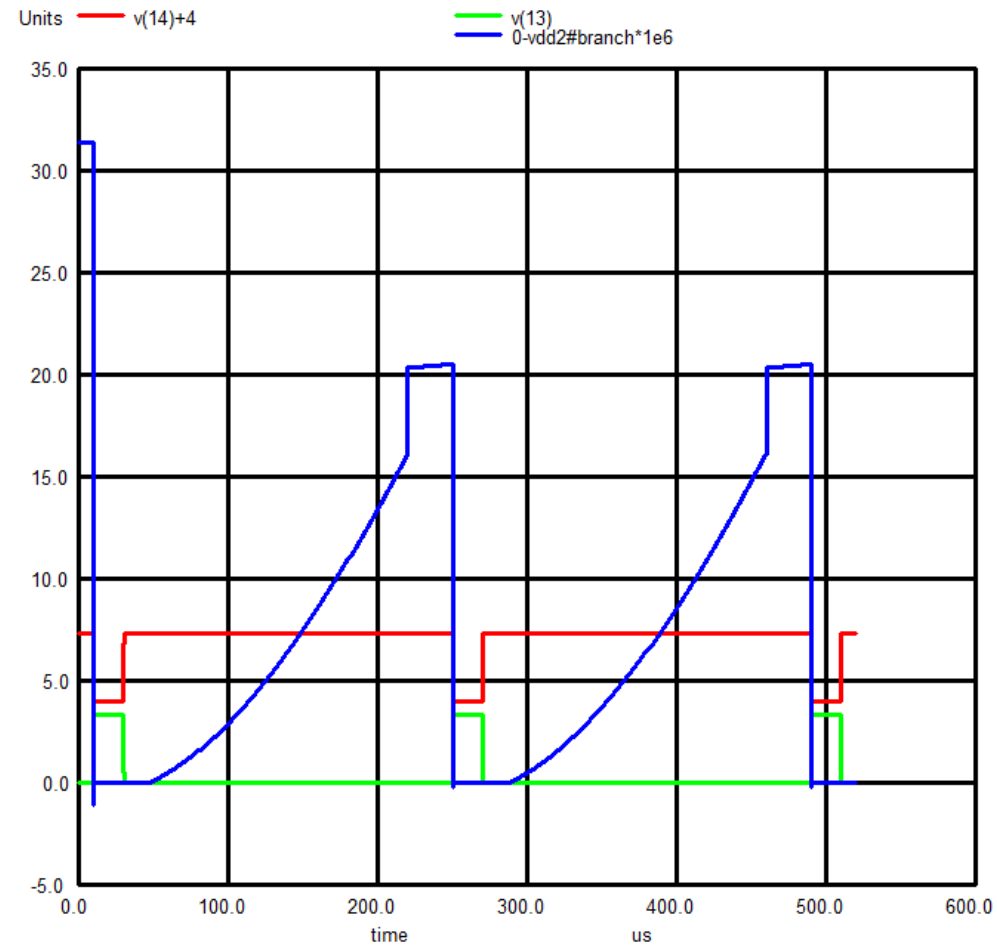


# PIXEL EM MODO DE CORRENTE

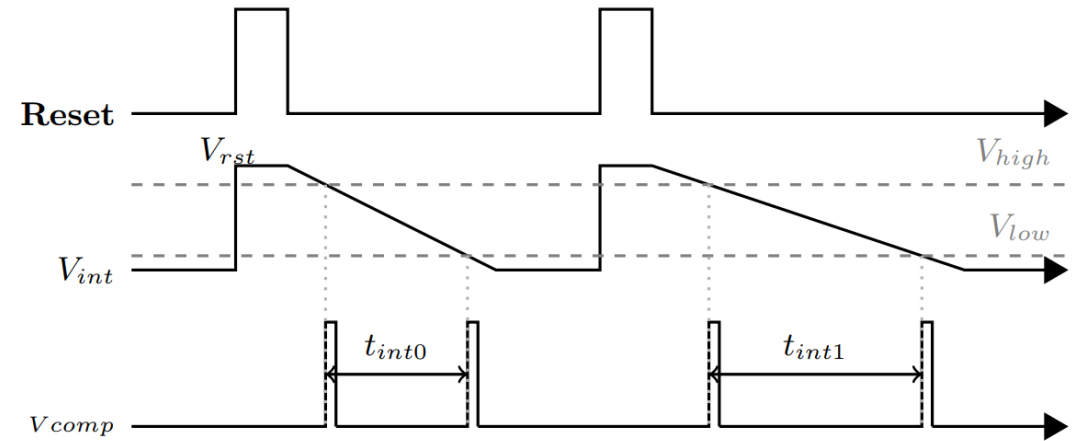
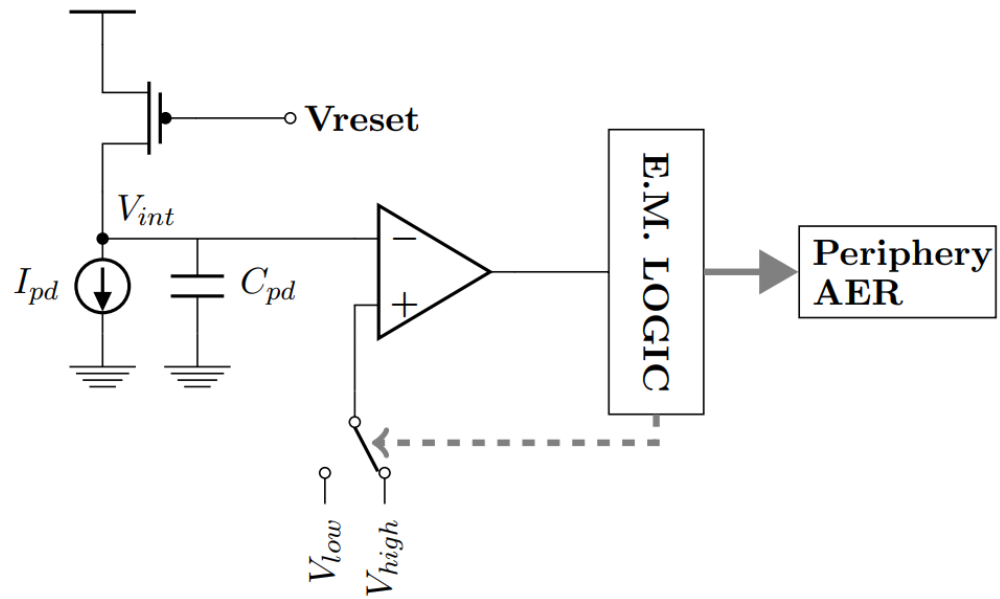


M1	11	12	1	0	MODN	W=1u	L=2u
M2	11	1	2	11	MODP	W=1u	L=3.7u
M3	2	2	0	0	MODN	W=2u	L=2u
M4	9	3	0	0	MODN	W=2u	L=2u
M5	10	4	0	0	MODN	W=2u	L=2u
M6	11	9	9	11	MODP	W=1u	L=2u
M7	11	9	10	11	MODP	W=1u	L=2u
M8	17	10	10	11	MODP	W=4u	L=2u
M9	2	13	3	0	MODN	W=1u	L=.35u
M10	3	14	3	0	MODN	W=0.5u	L=.35u
M11	2	14	3	11	MODP	W=1u	L=.35u
M12	3	13	3	11	MODP	W=0.5u	L=.35u
M13	2	15	4	0	MODN	W=1u	L=.35u
M14	4	16	4	0	MODN	W=0.5u	L=.35u
M15	2	16	4	11	MODP	W=1u	L=.35u
M16	4	15	4	11	MODP	W=0.5u	L=.35u
CP	1	0				10f	
IP	1	0				200p	
VDD	11	0				3.3	
VR	12	0				PULSE 0 3.3	10u 100n 100n 10u 240u
VP1	13	0				PULSE 0 3.3	10u 100n 100n 20u 240u
VP1b	14	0				PULSE 3.3 0	10u 100n 100n 20u 240u
VP2	15	0				PULSE 0 3.3	10u 100n 100n 210u 240u
VP2b	16	0				PULSE 3.3 0	10u 100n 100n 210u 240u
VDD2	17	0				3.3	

# PIXEL EM MODO DE CORRENTE

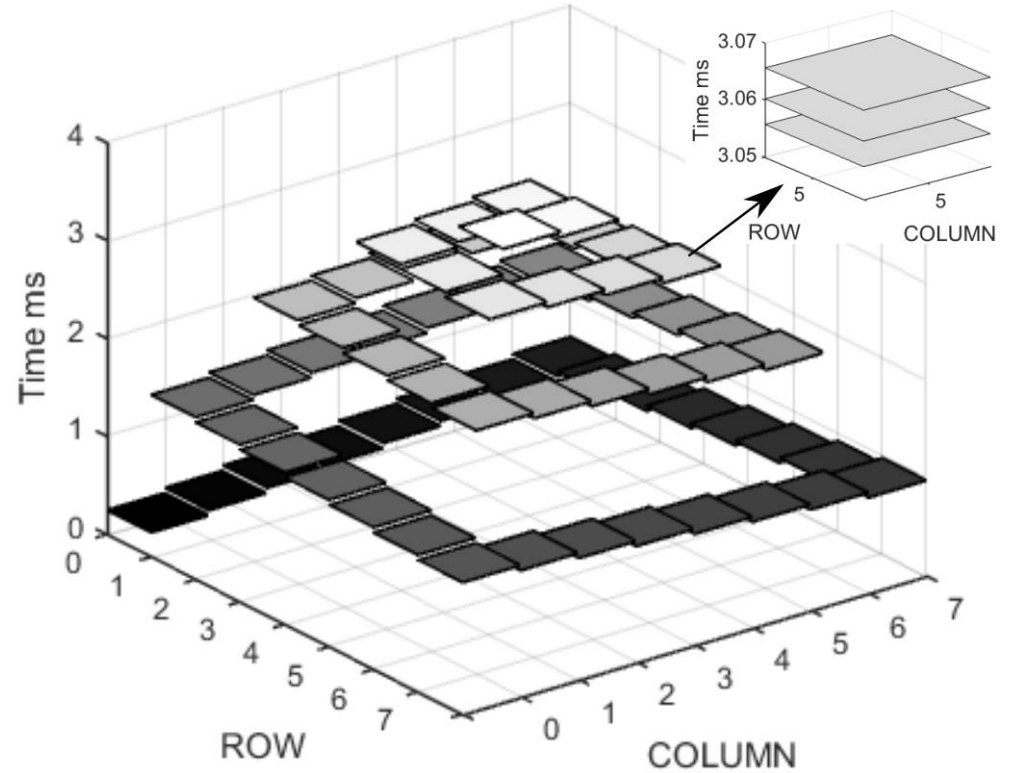
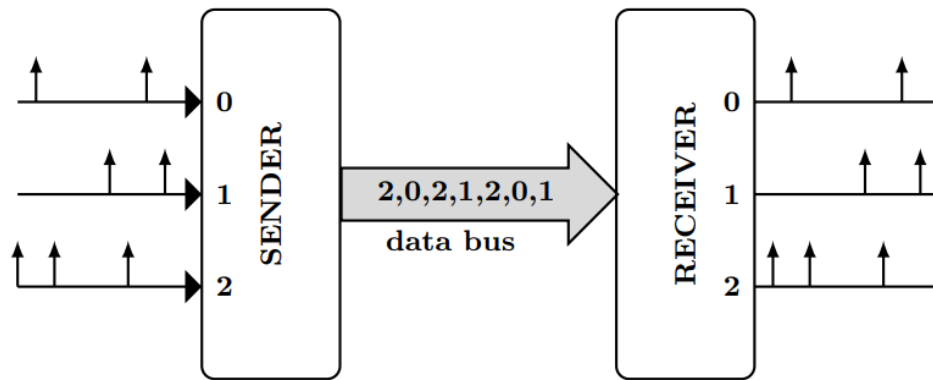


# PIXEL PULSADO

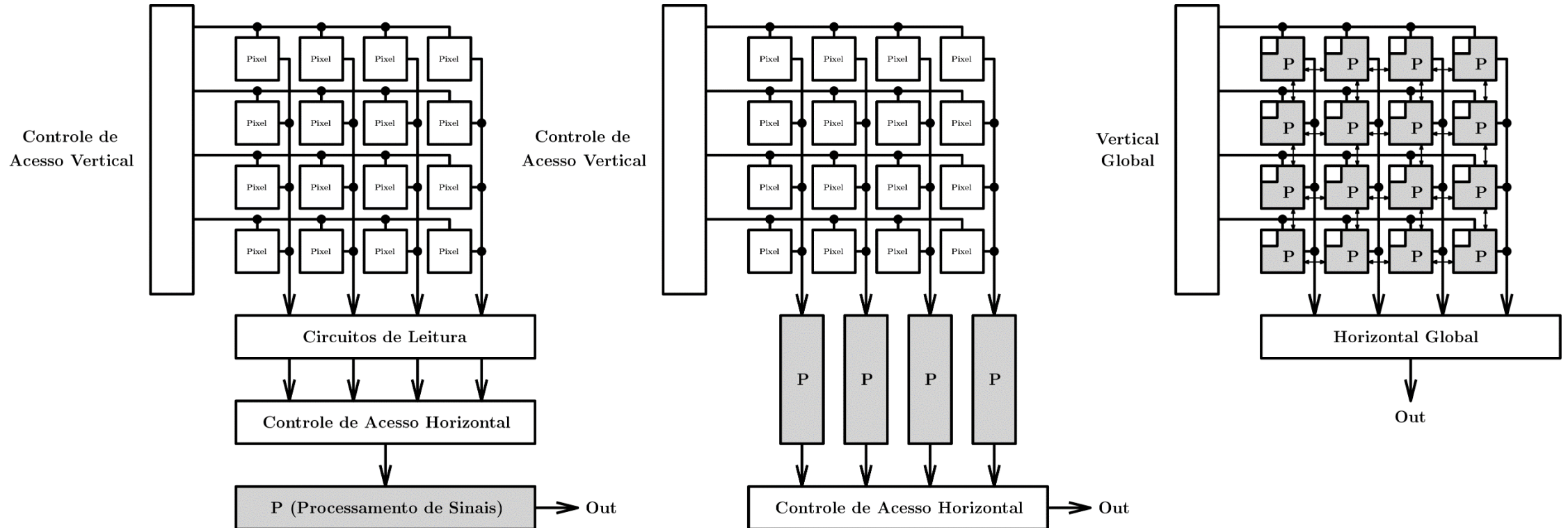




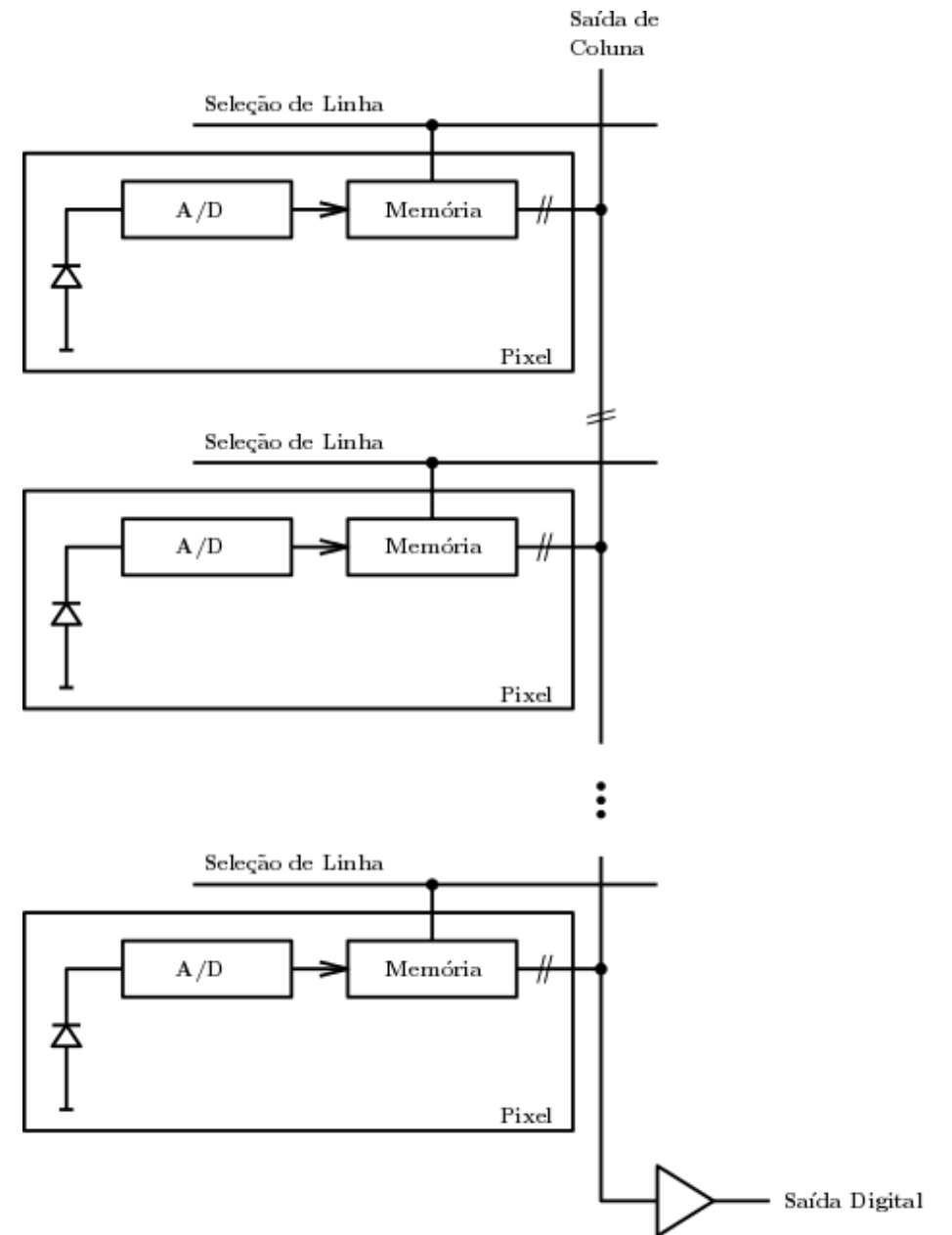
# PIXEL PULSADO



# PROCESSAMENTO DE IMAGENS NO PLANO FOCAL



# CONVERSÃO A/D NO PIXEL



# CONCLUSÕES

- **Pixels básicos: 3T, logarítmico, 4T, modo de corrente, pulsado**
- **Processamento de imagens no plano focal (tipos)**
- **“Address-event representations” (AER), processamento de sinais “biomórficos”**
- **Visão computacional e redes neurais, aproveitando o paralelismo intrínseco**

# REFERÊNCIAS

- **J. Ohta, Smart CMOS Image Sensors and Applications, CRC Press, 2007.**
- **J. Nakamura (Editor), Image Sensors and Signal Processing for Digital Still Cameras, CRC Press, 2005.**
- **G. C. Holst e T. S. Lomheim, CMOS/CCD Sensors and Camera Systems, JCD Publishing and SPIE Press, 2007.**
- **A. N. Belbachir (Editor), Smart Cameras, Springer, 2010.**
- **T. Kuroda, Essential Principles of Image Sensors, CRC Press, 2017.**
- **S. Kleinfelder, S. Lim, X. Liu e A. El Gamal, A 10000 Frames/s CMOS Digital Pixel Sensor, IEEE J. Solid-State Circuits, vol. 36, no. 12, pp. 2049-2059, Dez. 2001.**
- **J. P. G. Ruiz, A Comparative Analysis of Dynamic Vision Sensors using 180 nm CMOS Technology, Dissertação de Mestrado, PEE/COPPE/UFRJ, 2017.**



**OBRIGADO!**

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# PROCESSAMENTO DE IMAGENS NO PLANO FOCAL

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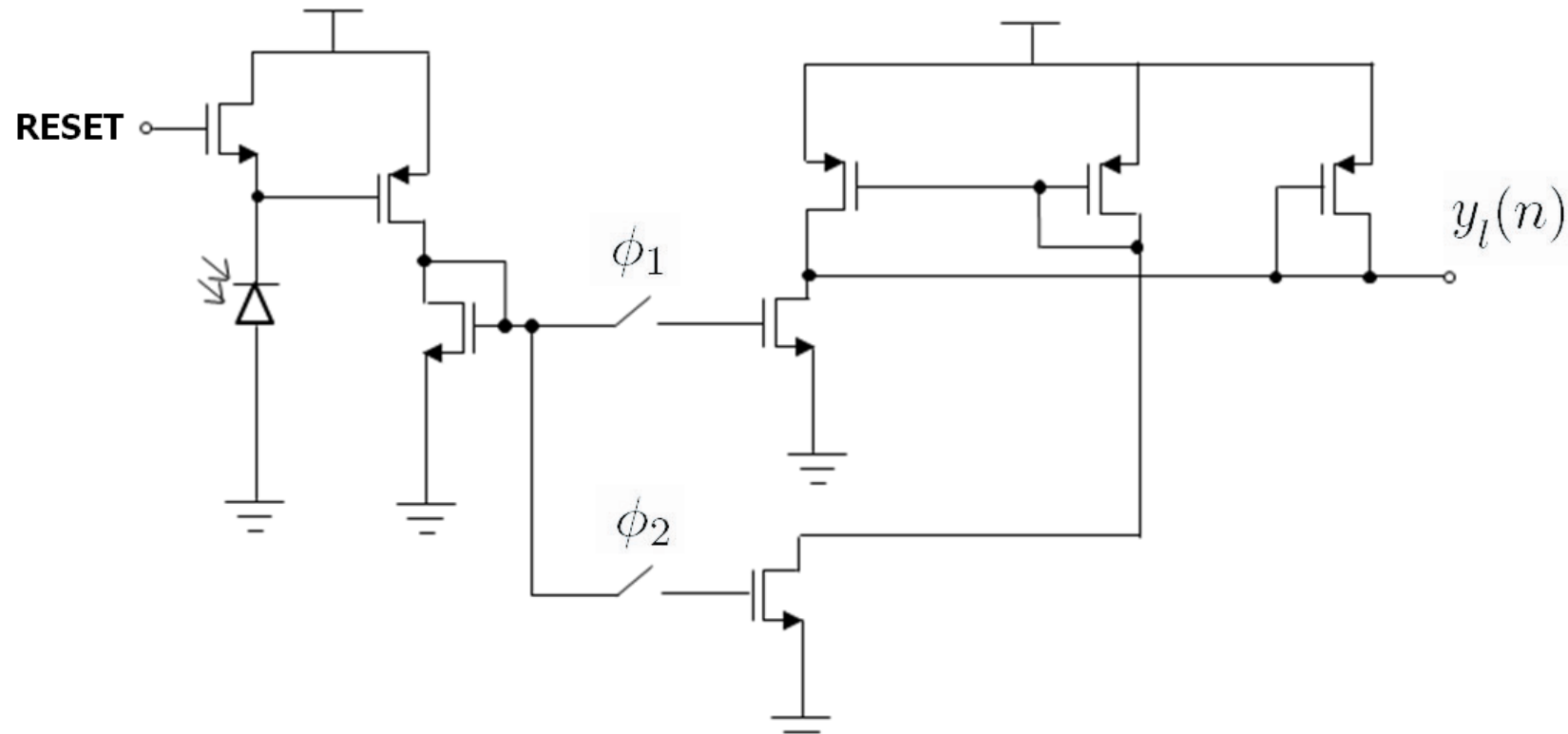
# CONTEÚDO

- **Pixel em Modo de Corrente**
- **Operações Básicas**
- **Aplicações e Exemplos**
- **Tendências Futuras**

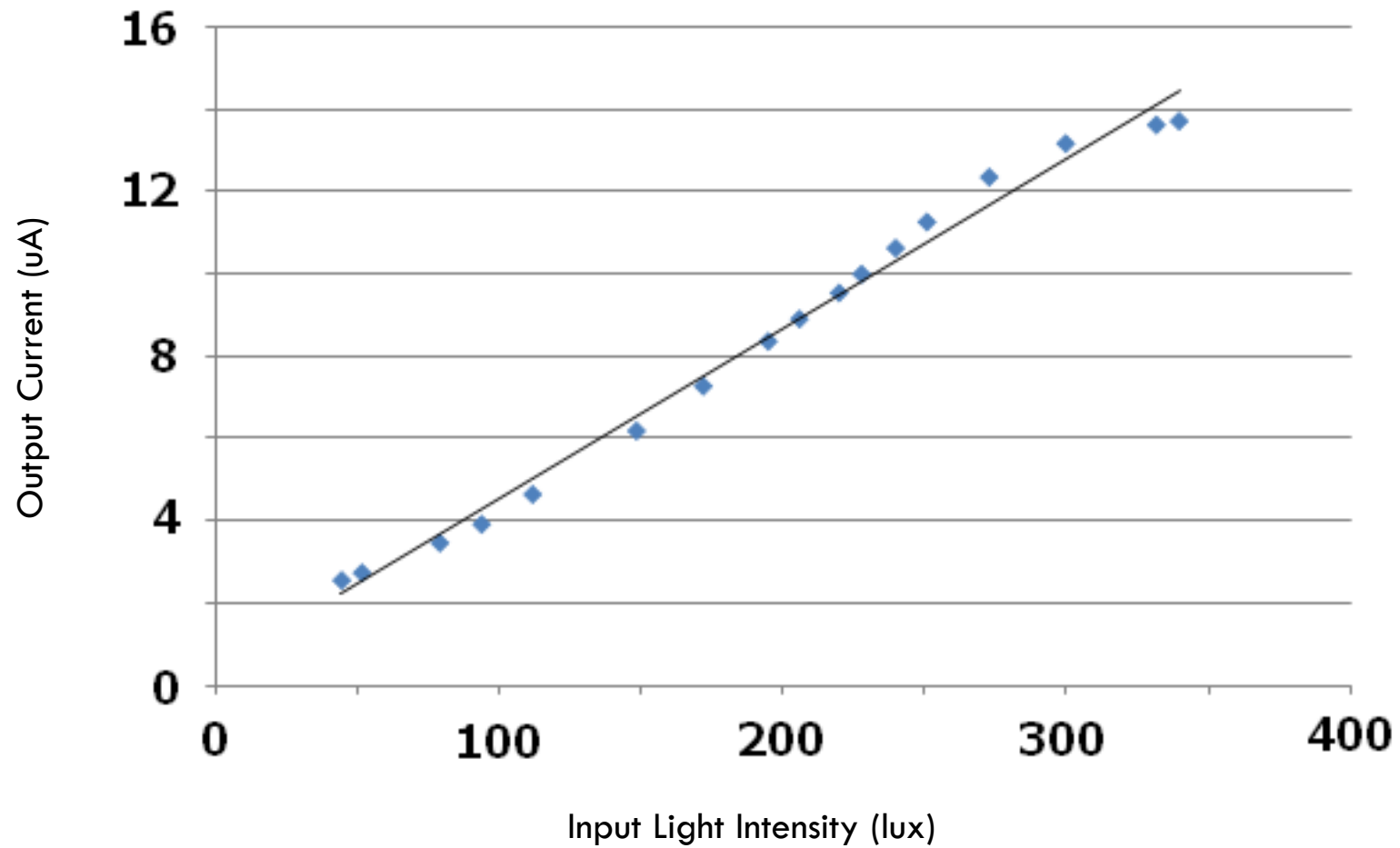


# PIXEL EM MODO DE CORRENTE

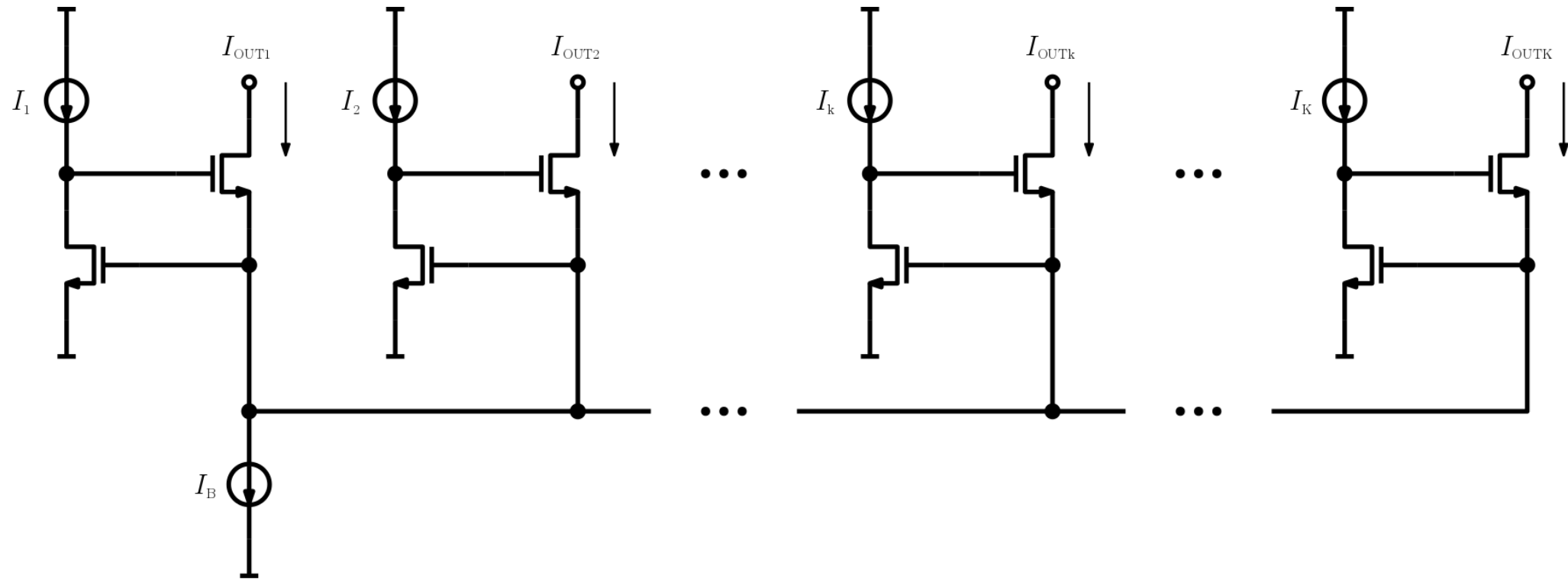
- Representação de sinais em modo adequado para execução de operações simples



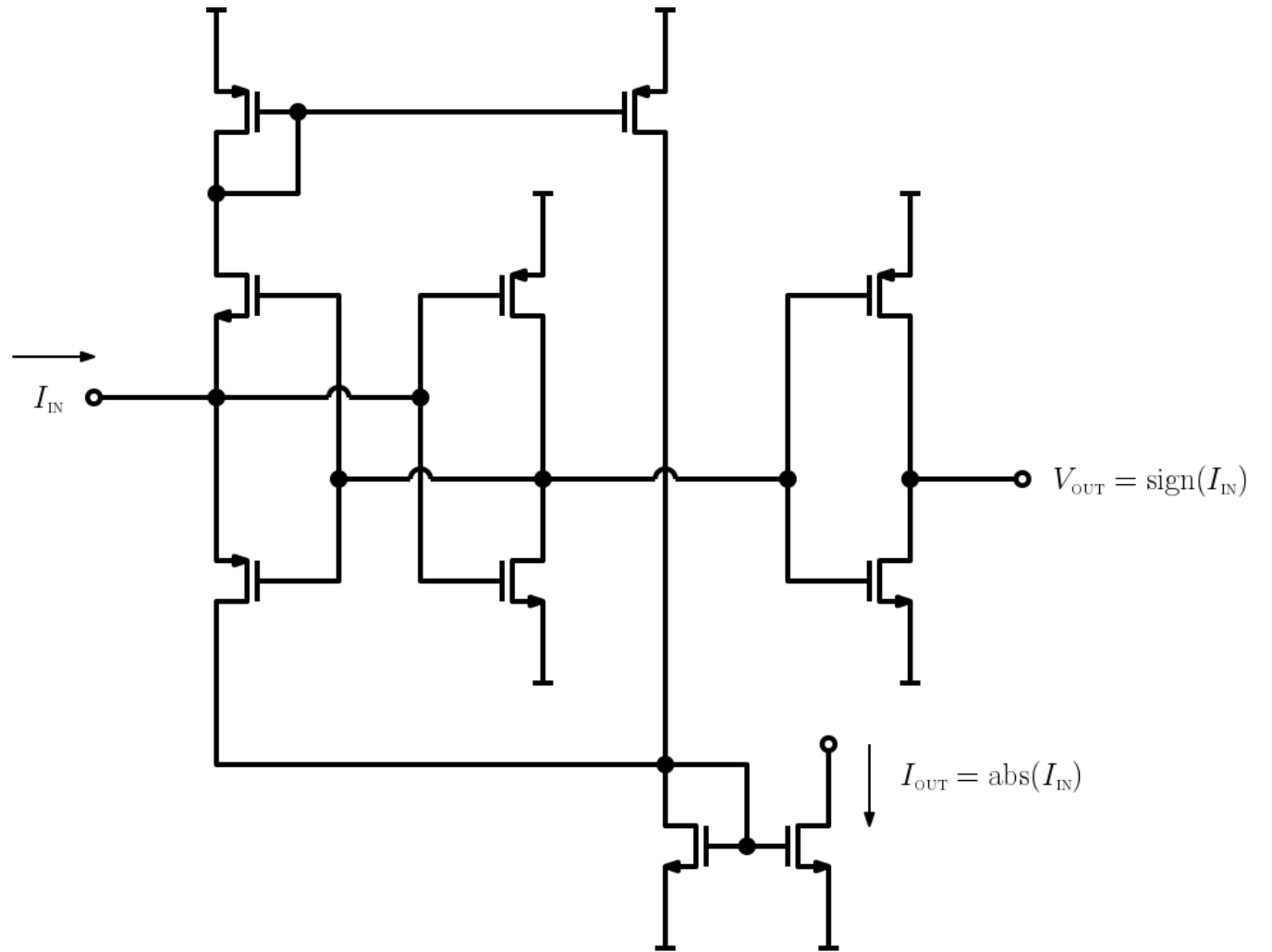
# PIXEL EM MODO DE CORRENTE



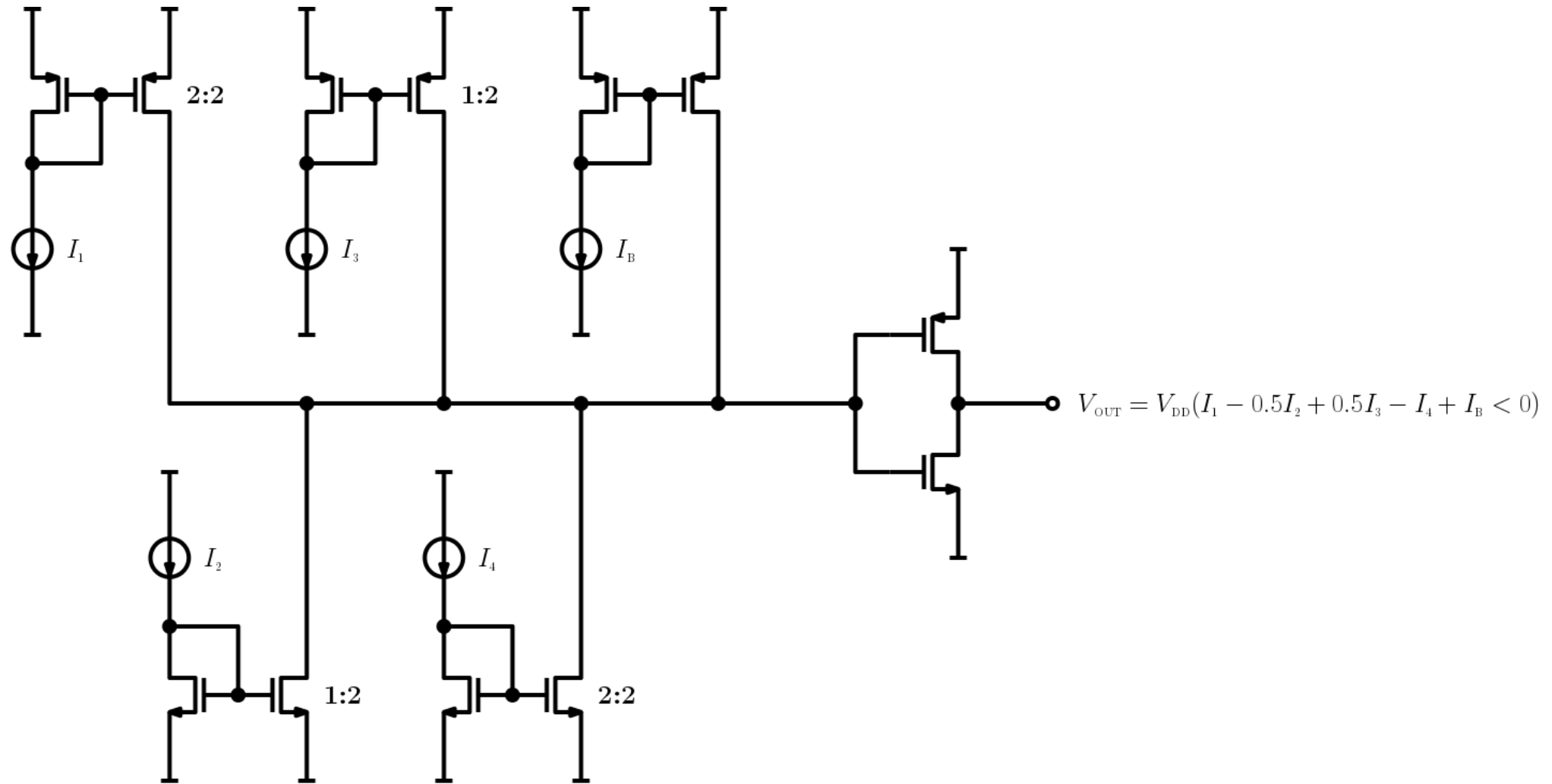
# WINNER TAKES ALL



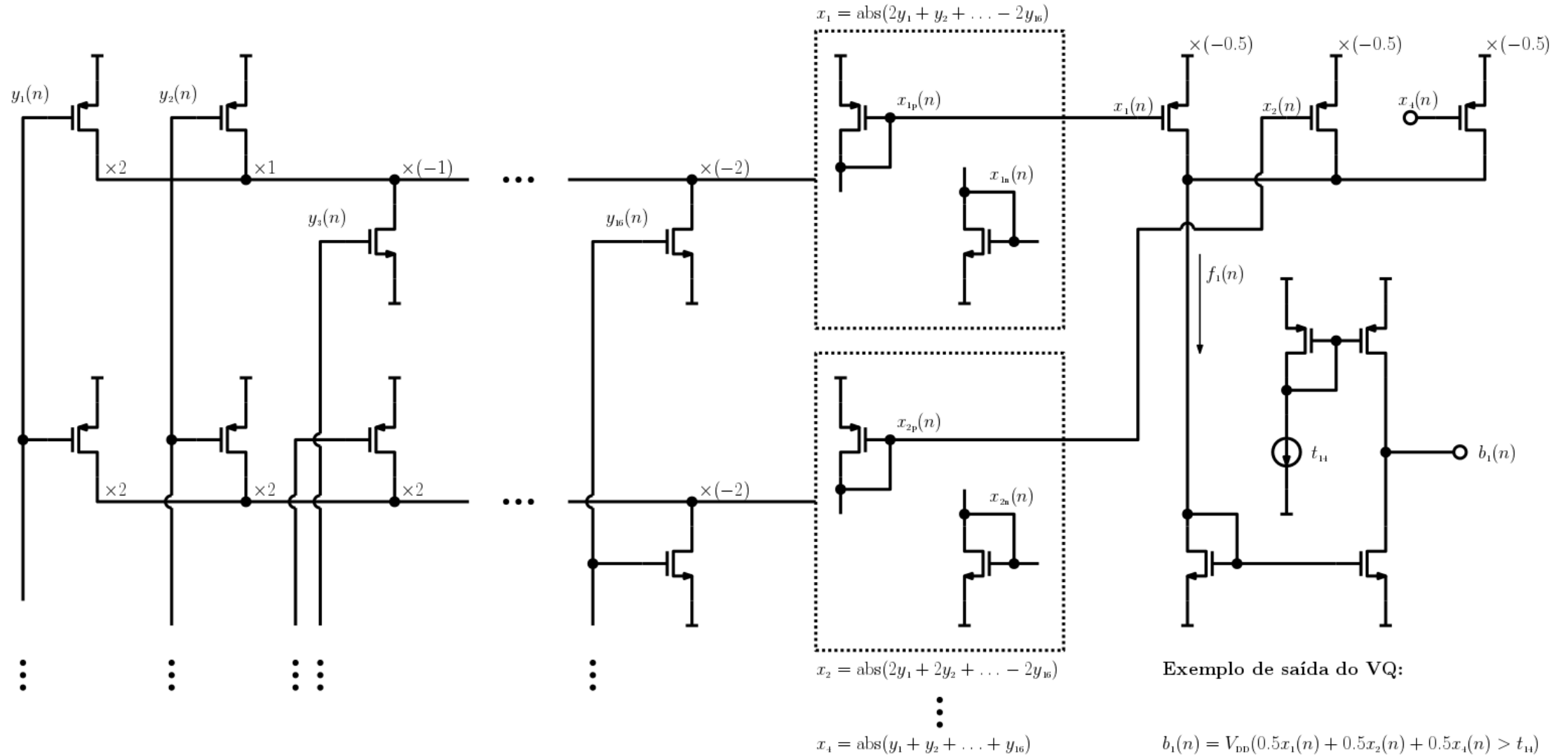
# VALOR ABSOLUTO



# PRODUTO INTERNO E COMPARADOR

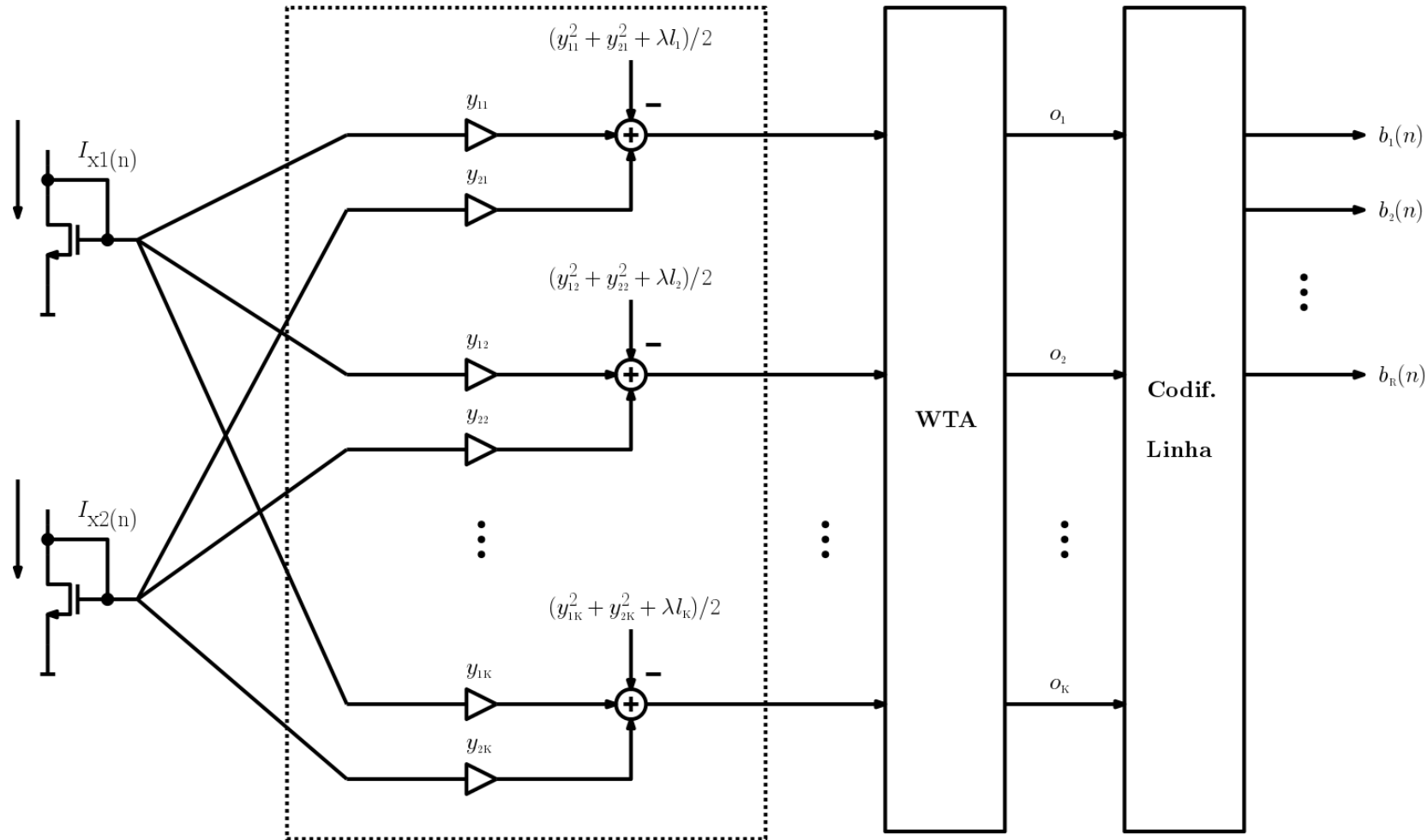


# TRANSFORMADA LINEAR

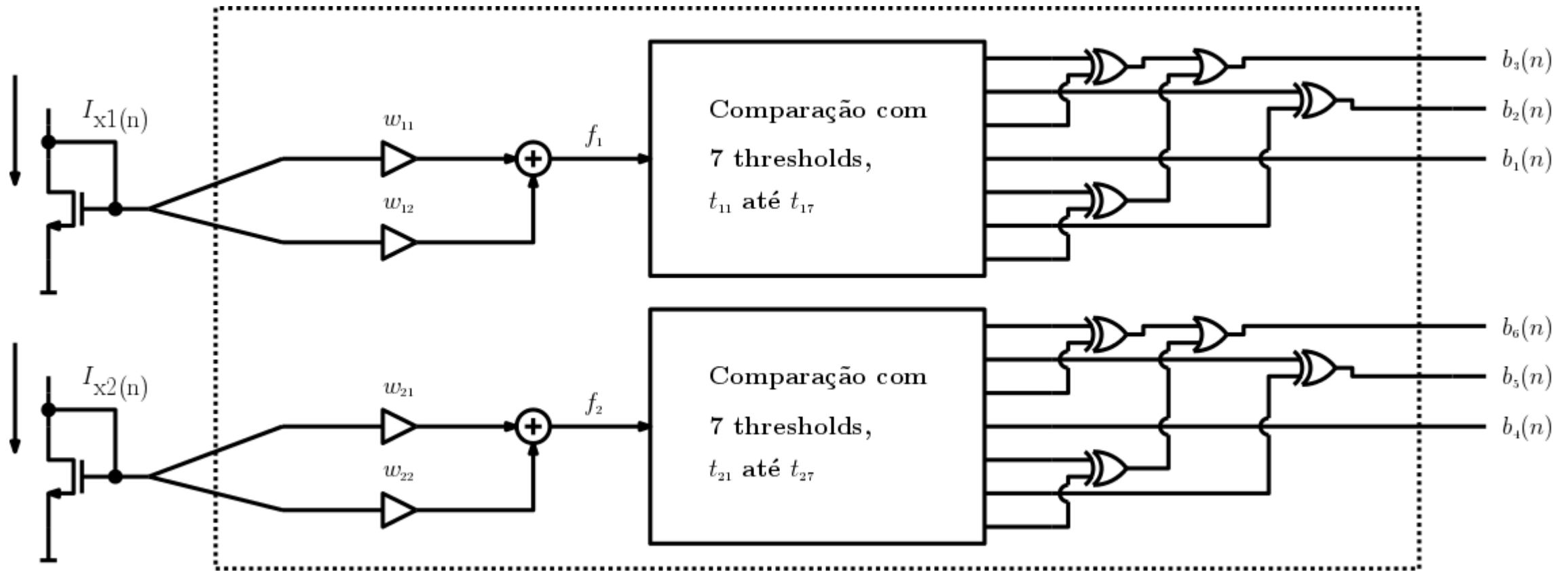


# VQ COM RESTRIÇÃO DE ENTROPIA (ECVQ)

$$i(n) = \operatorname{argmin}_k (d(\mathbf{x}(n), \mathbf{y}_k) + \lambda l_k) = \operatorname{argmax}_k (-\mathbf{x}^T(n)\mathbf{x}(n) + 2\mathbf{x}^T\mathbf{y}_k - \mathbf{y}_j^T\mathbf{y}_k - \lambda l_k)$$

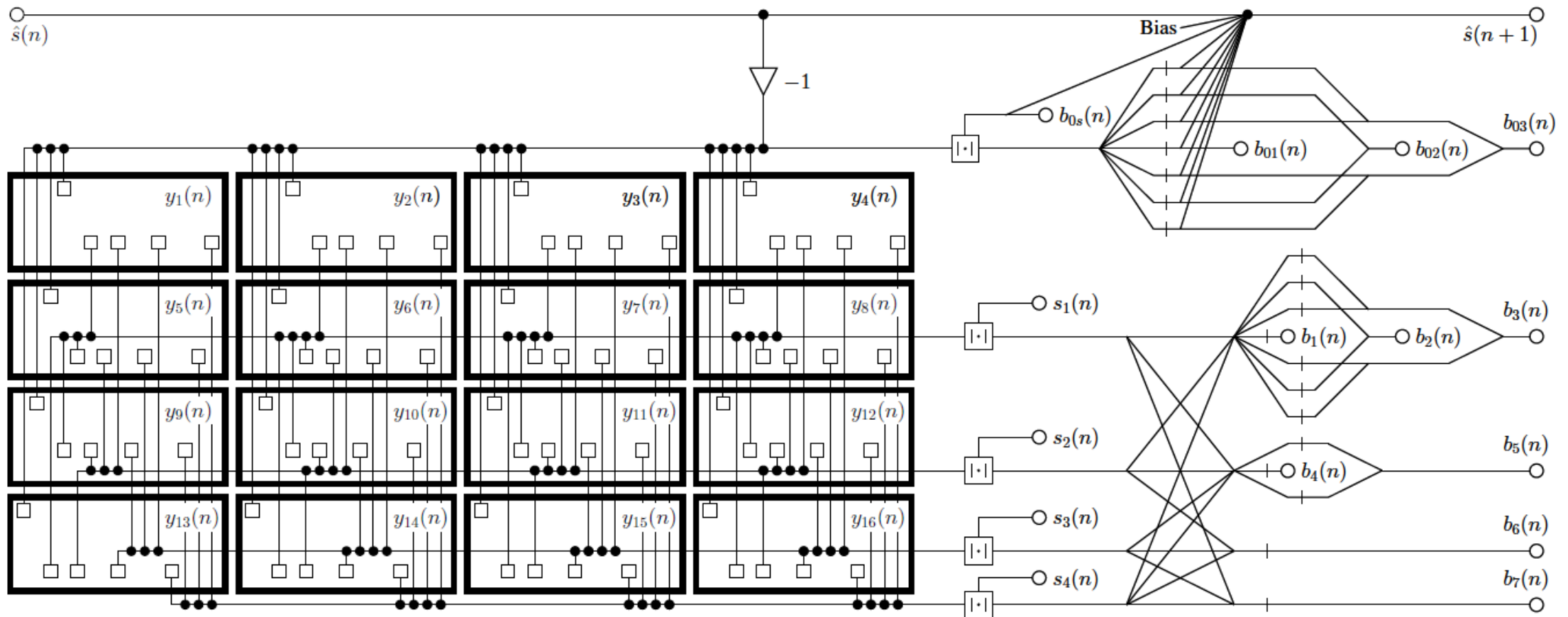


# ECVQ COM RESTRIÇÃO DE COMPLEXIDADE

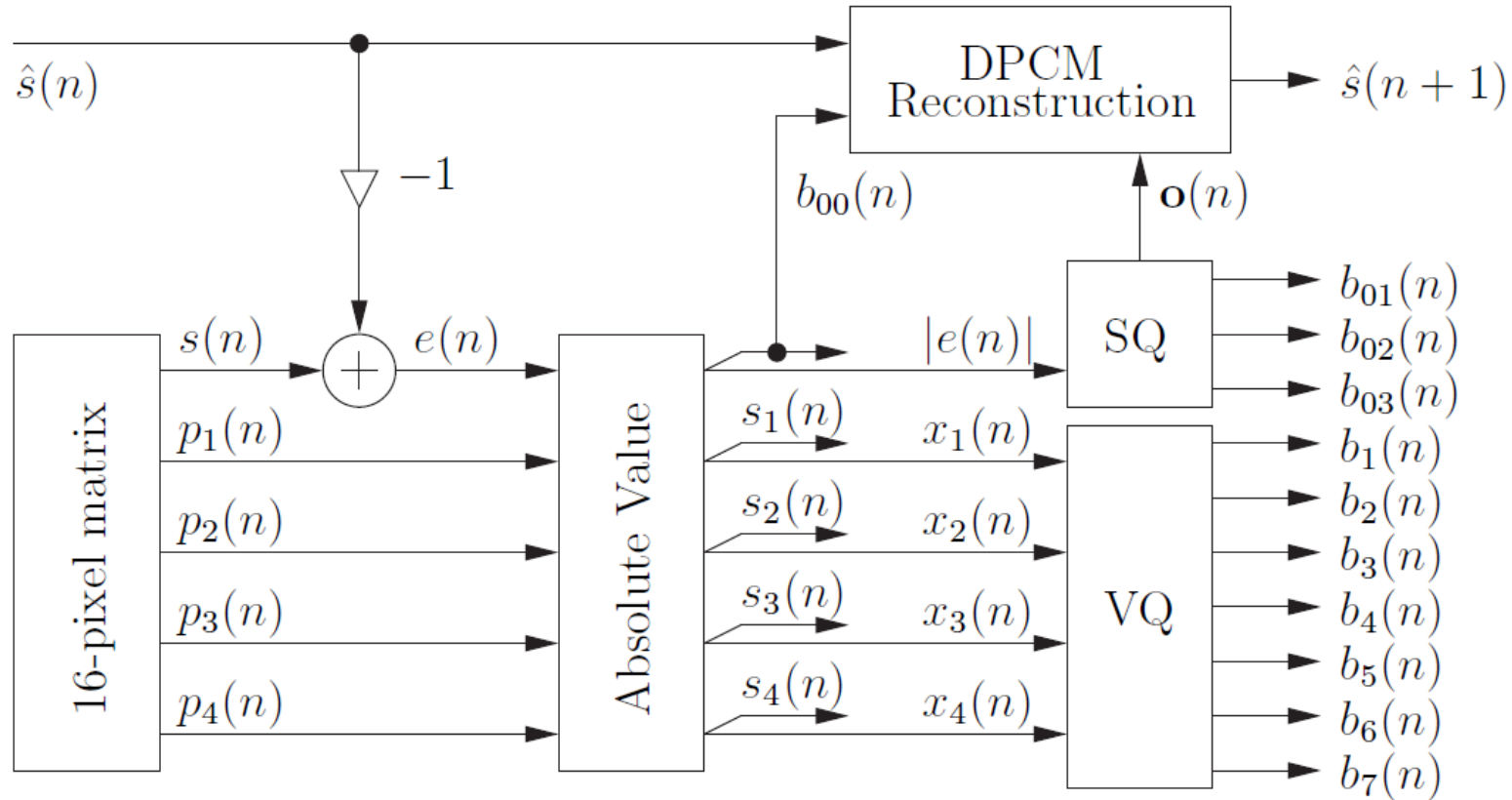




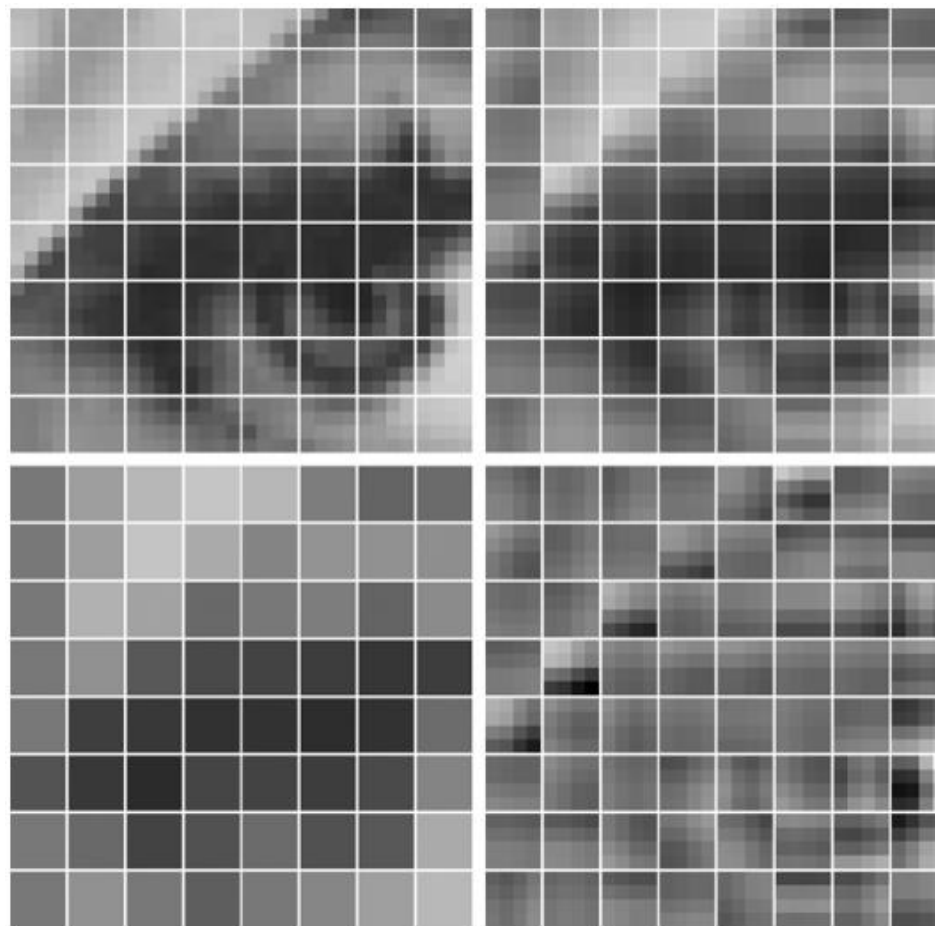
# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL



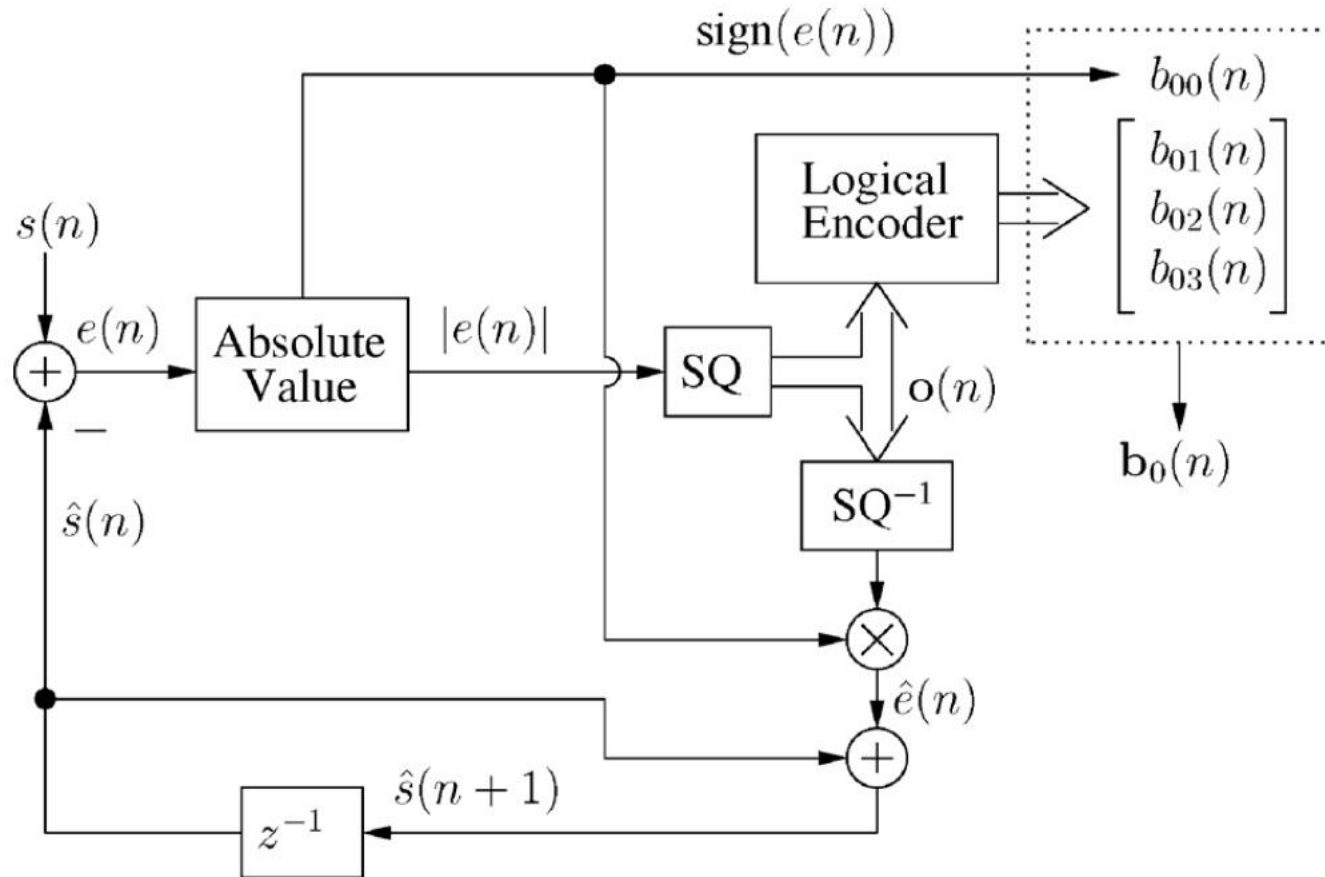
# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL



# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL

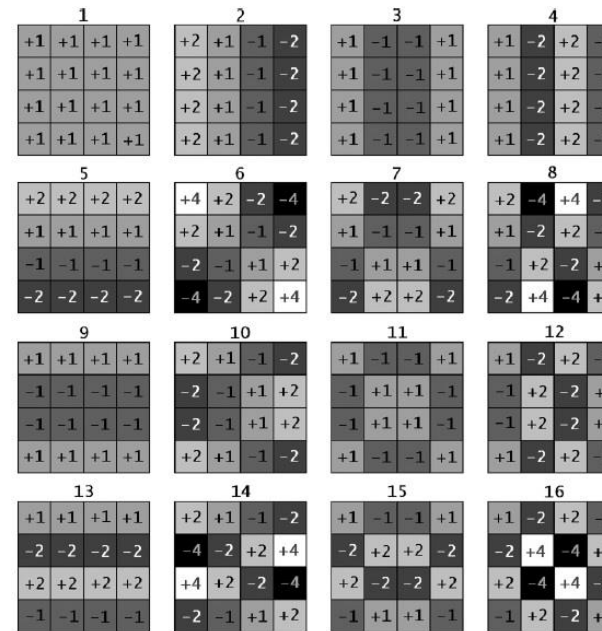


# DIFFERENTIAL PULSE-CODE MODULATION



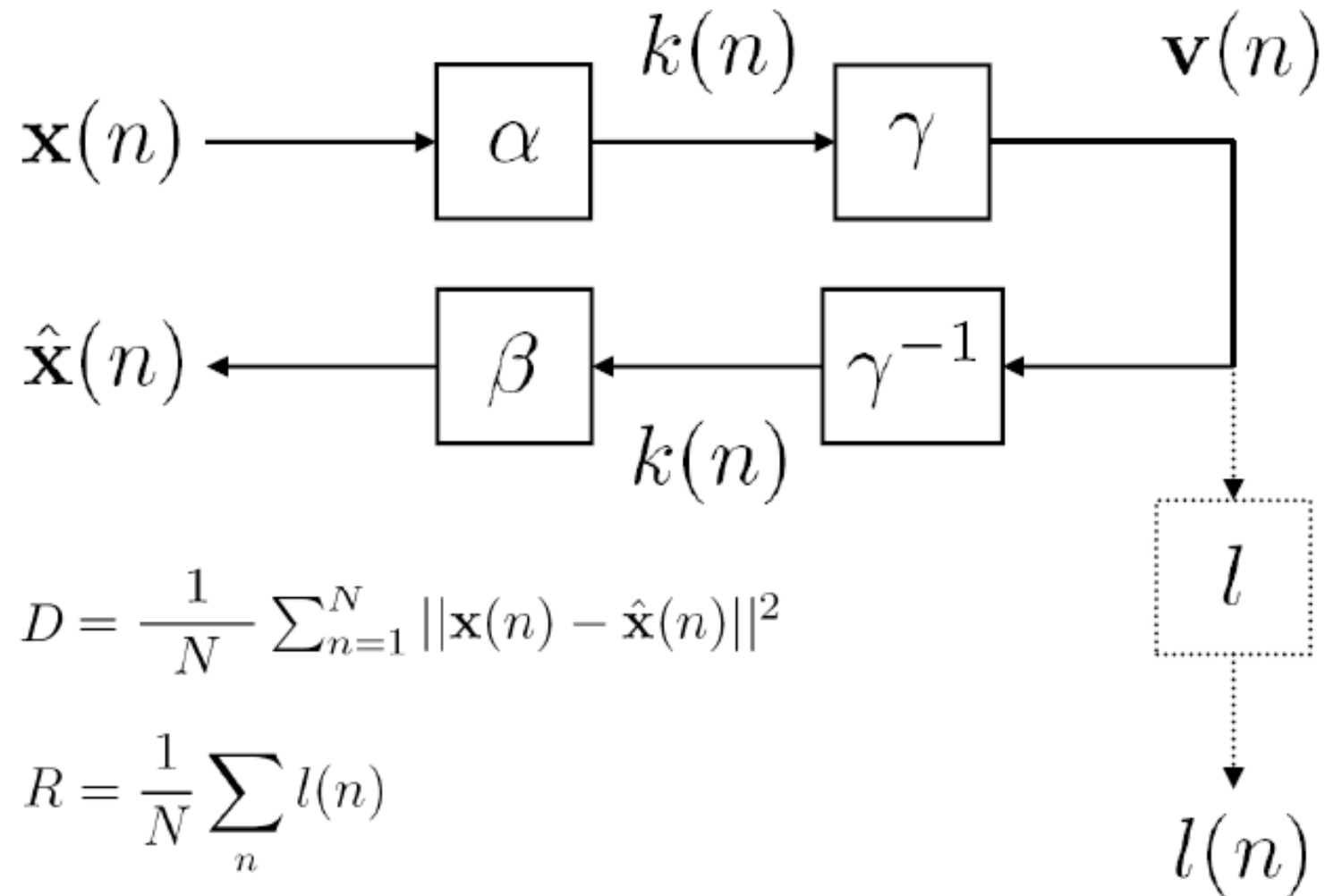
# REPRESENTAÇÃO DOMÍNIO TRANSFORMADA

$$H^T = \begin{bmatrix} 2 & 2 & 1 & 1 \\ 1 & 2 & -1 & 1 \\ -1 & 2 & -1 & 1 \\ -2 & 2 & 1 & 1 \\ 2 & 1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ -1 & 1 & -1 & -1 \\ -2 & 1 & 1 & -1 \\ 2 & -1 & 1 & -1 \\ 1 & -1 & -1 & -1 \\ -1 & -1 & -1 & -1 \\ -2 & -1 & 1 & -1 \\ 2 & -2 & 1 & 1 \\ 1 & -2 & -1 & 1 \\ -1 & -2 & -1 & 1 \\ -2 & -2 & 1 & 1 \end{bmatrix}$$

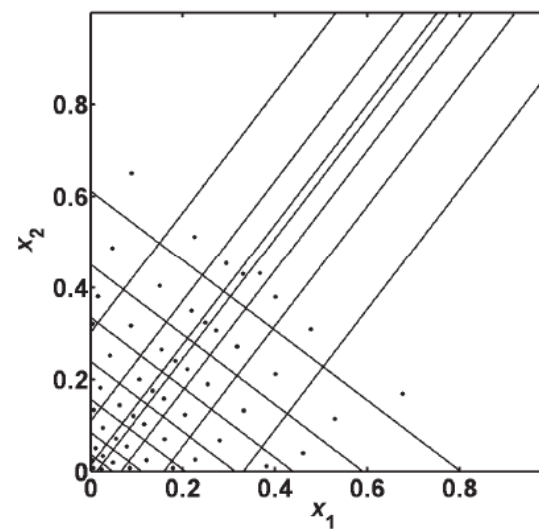
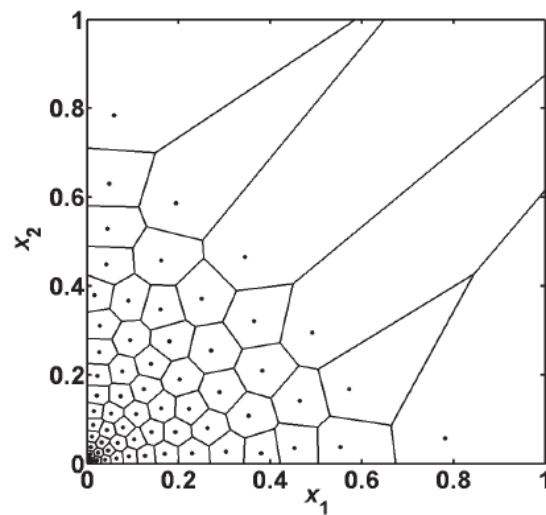
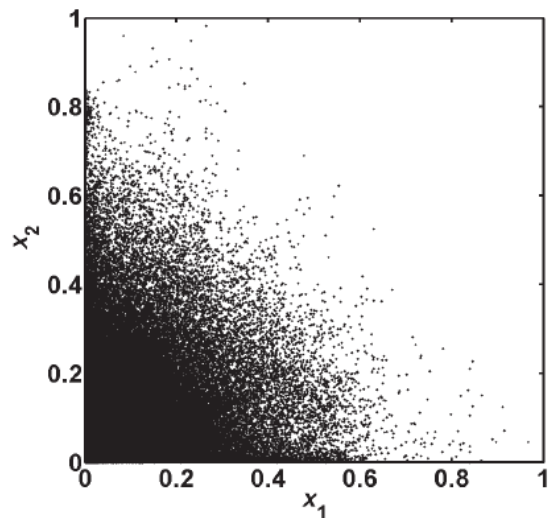


<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>
<b>5</b>	<b>6</b>	<b>7</b>	<b>8</b>
<b>9</b>	<b>10</b>	<b>11</b>	<b>12</b>
<b>13</b>	<b>14</b>	<b>15</b>	<b>16</b>

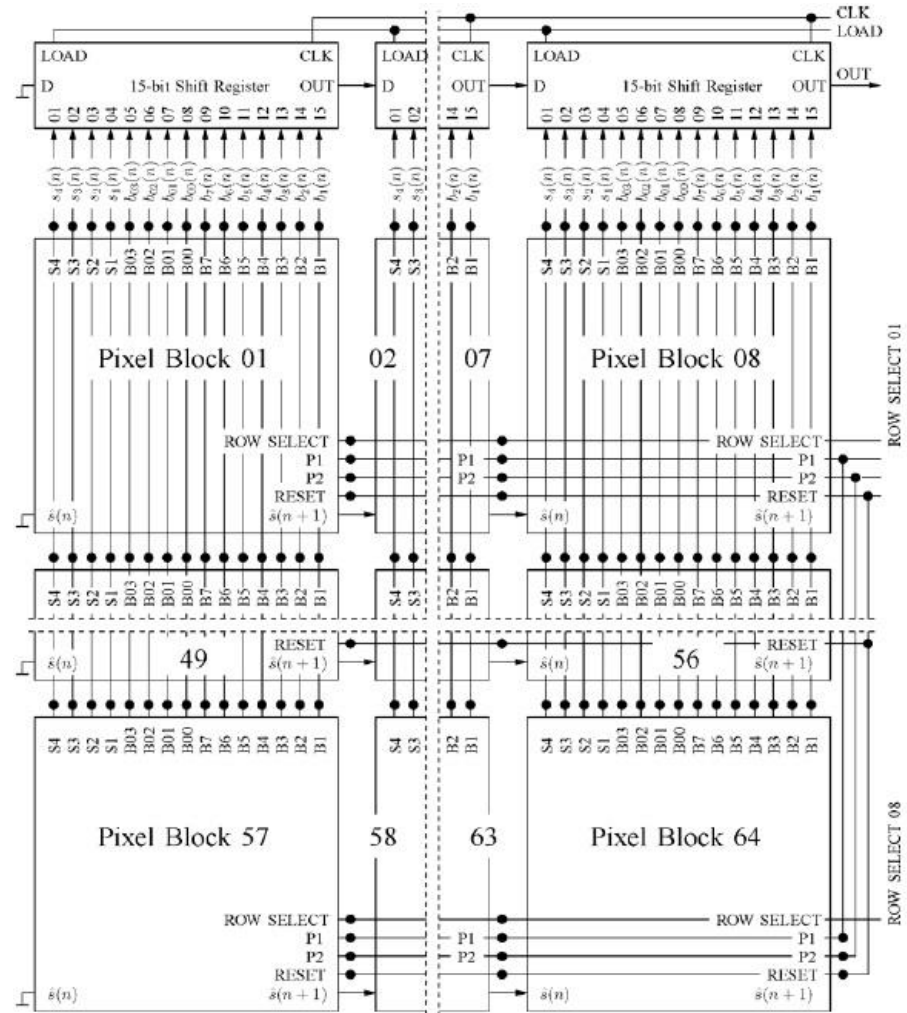
# QUANTIZAÇÃO VETORIAL



# IMPLEMENTAÇÃO DO VQ

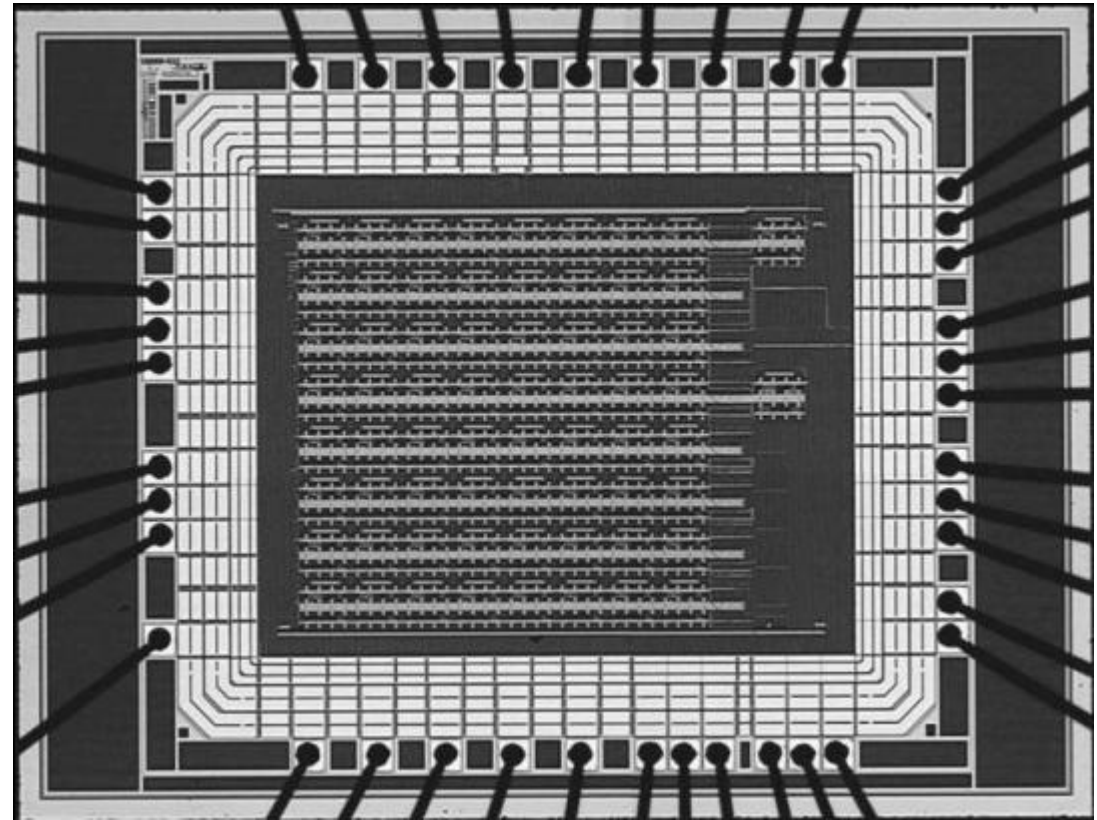
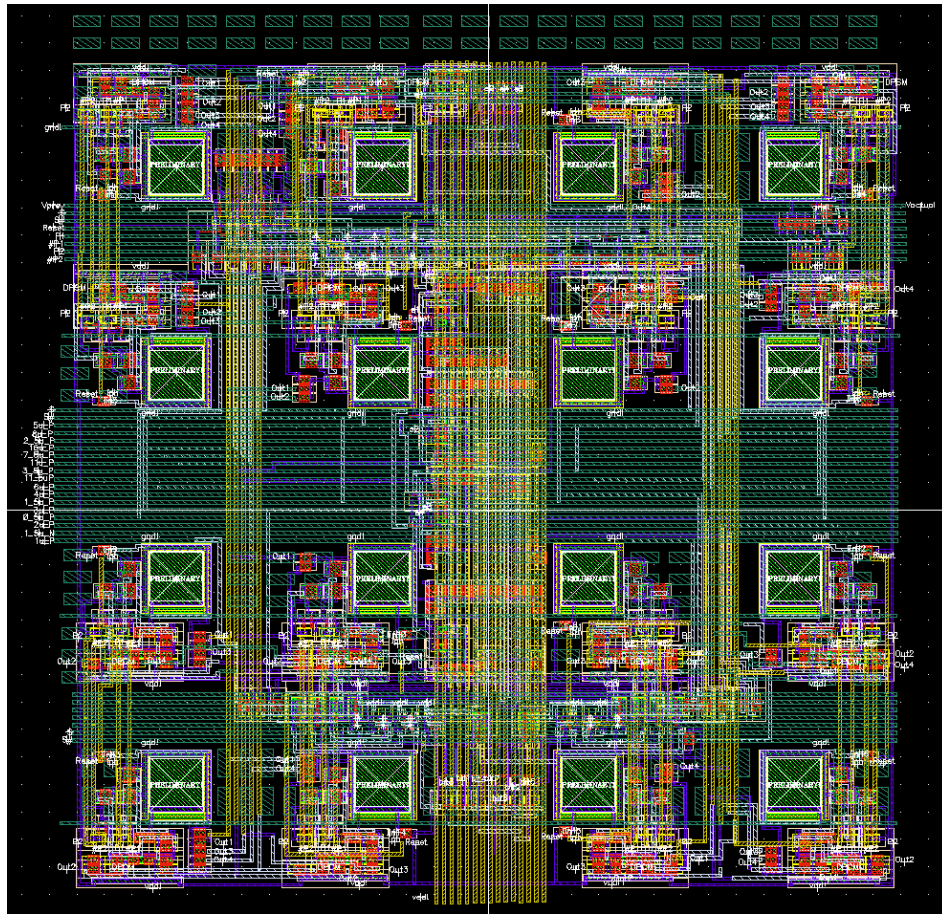


# LAYOUT COMPLETE

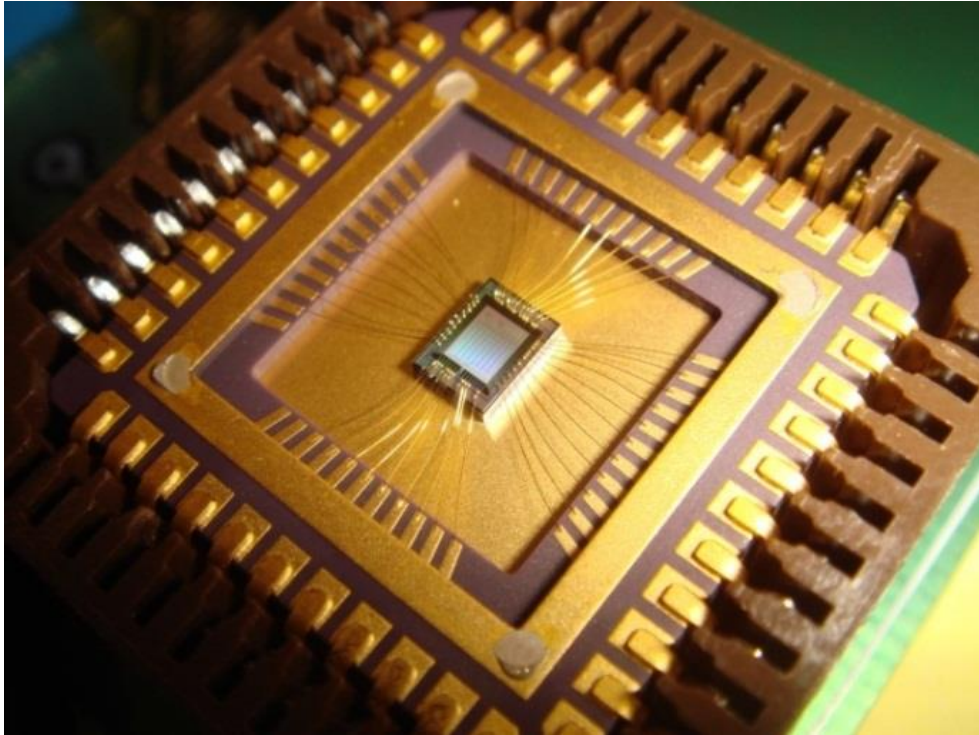




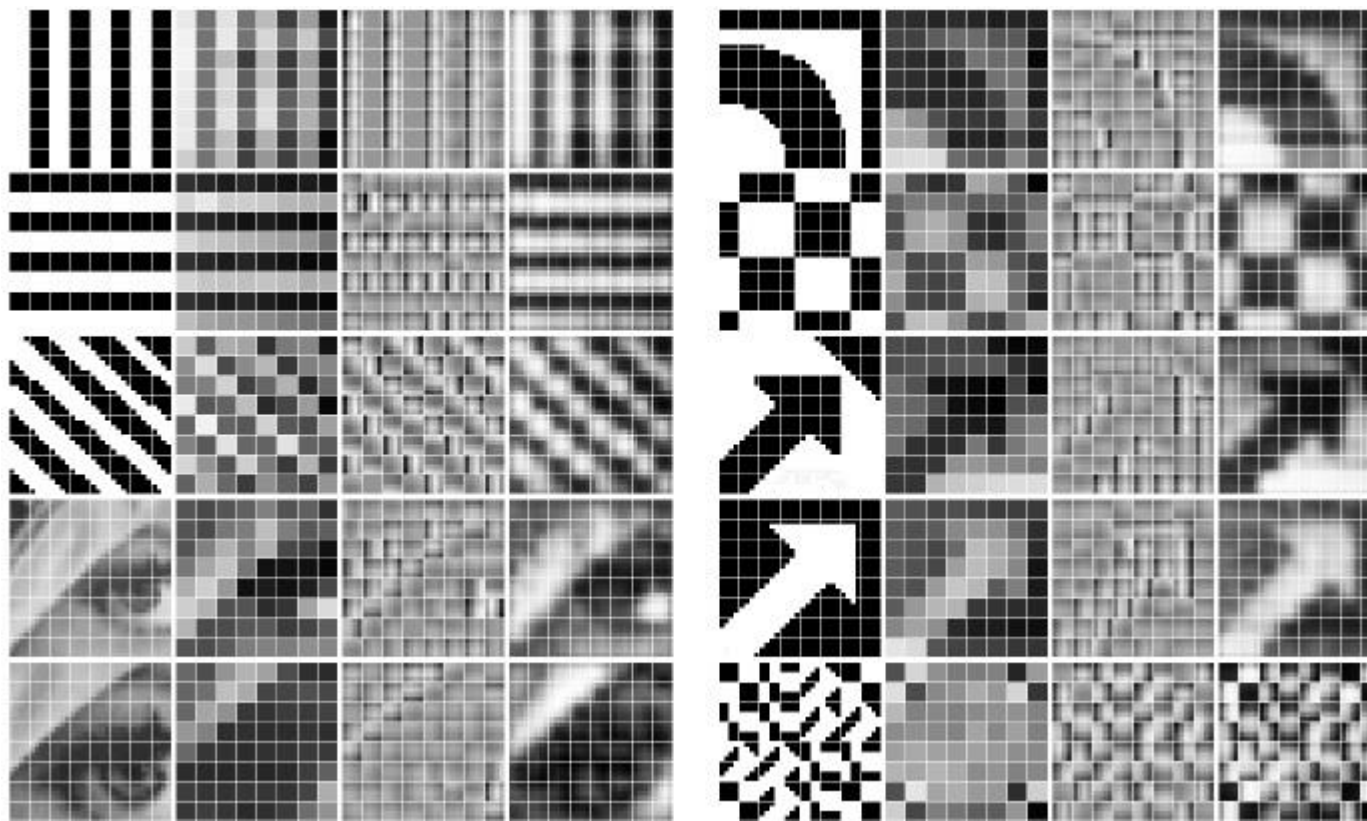
# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL



# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL



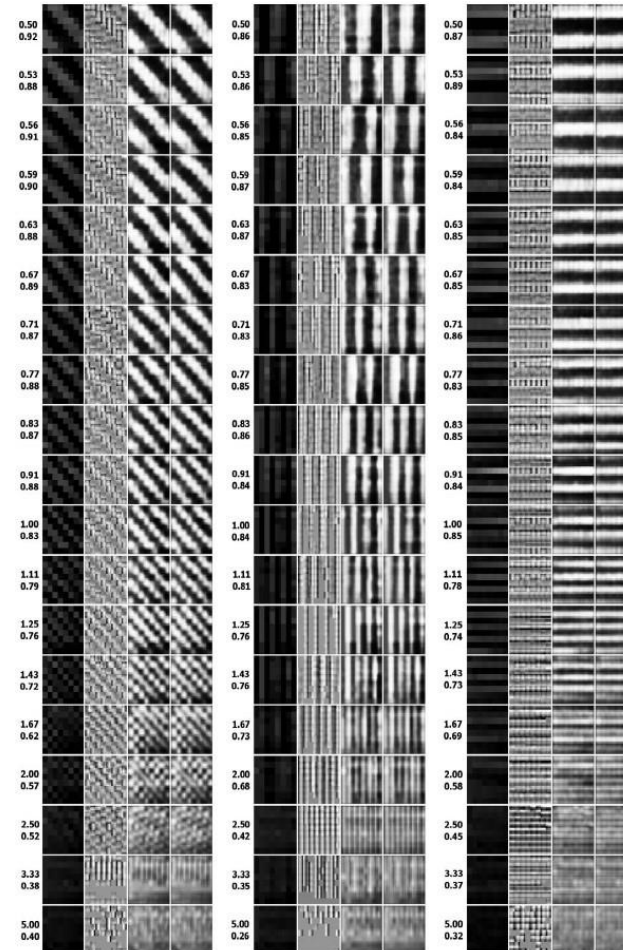
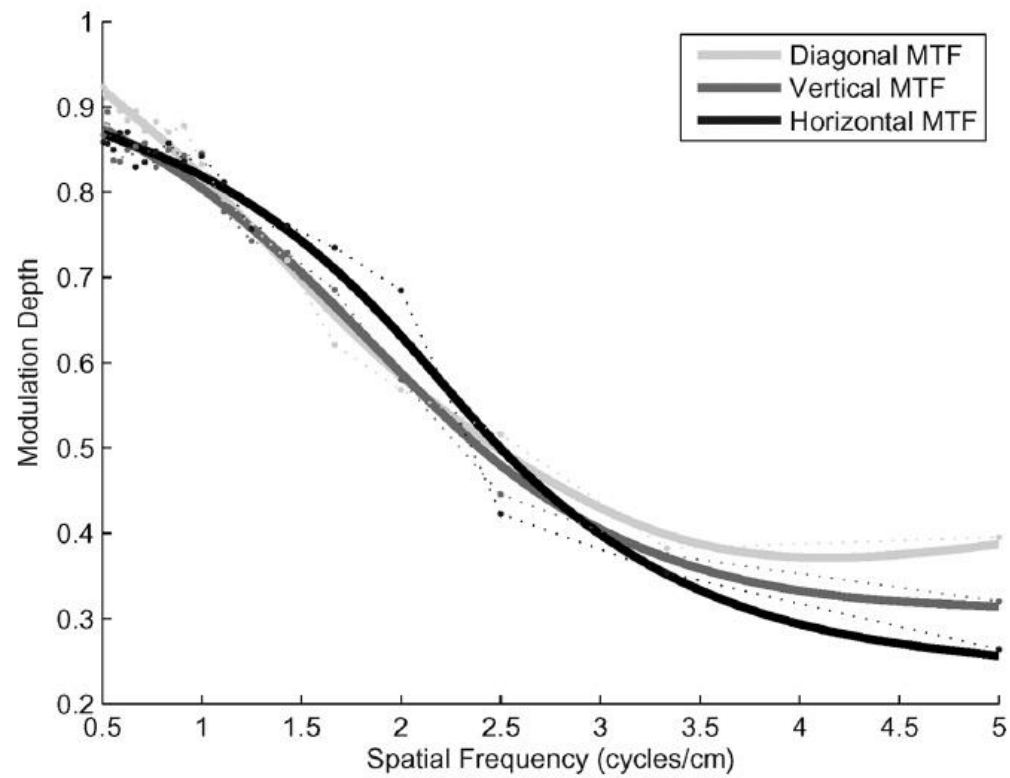
# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL



# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL



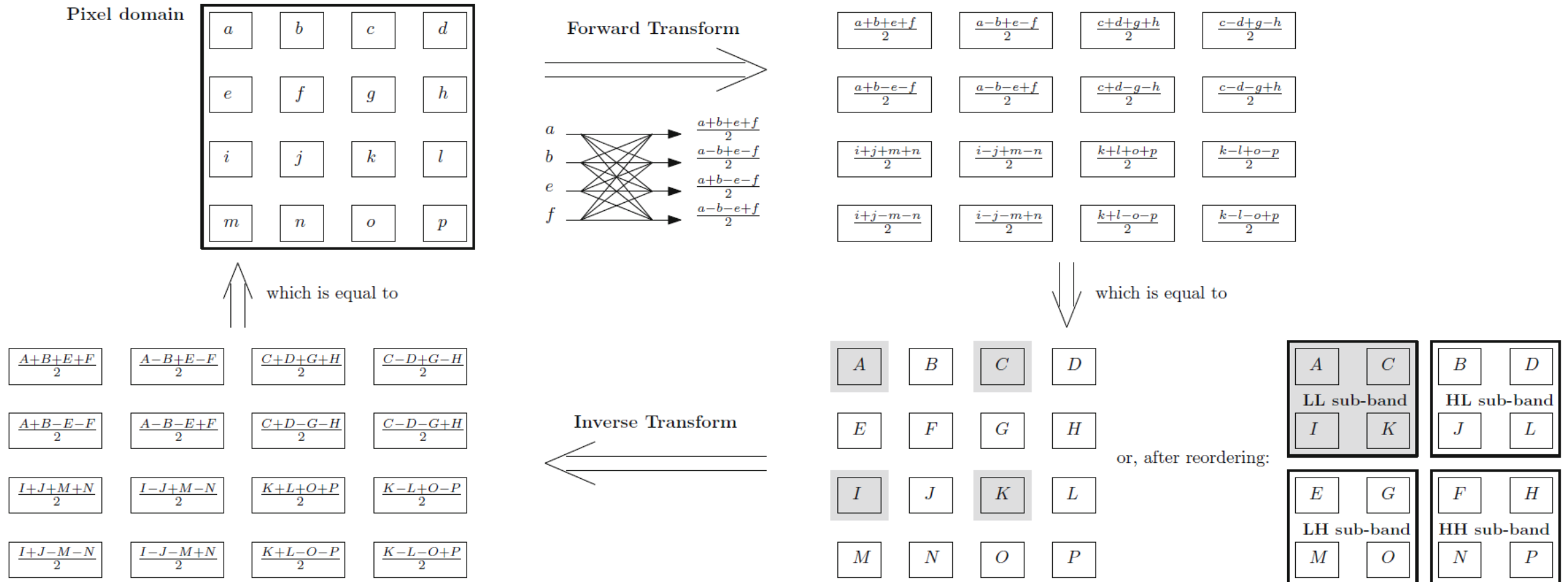
# MODULATION TRANSFER FUNCTION



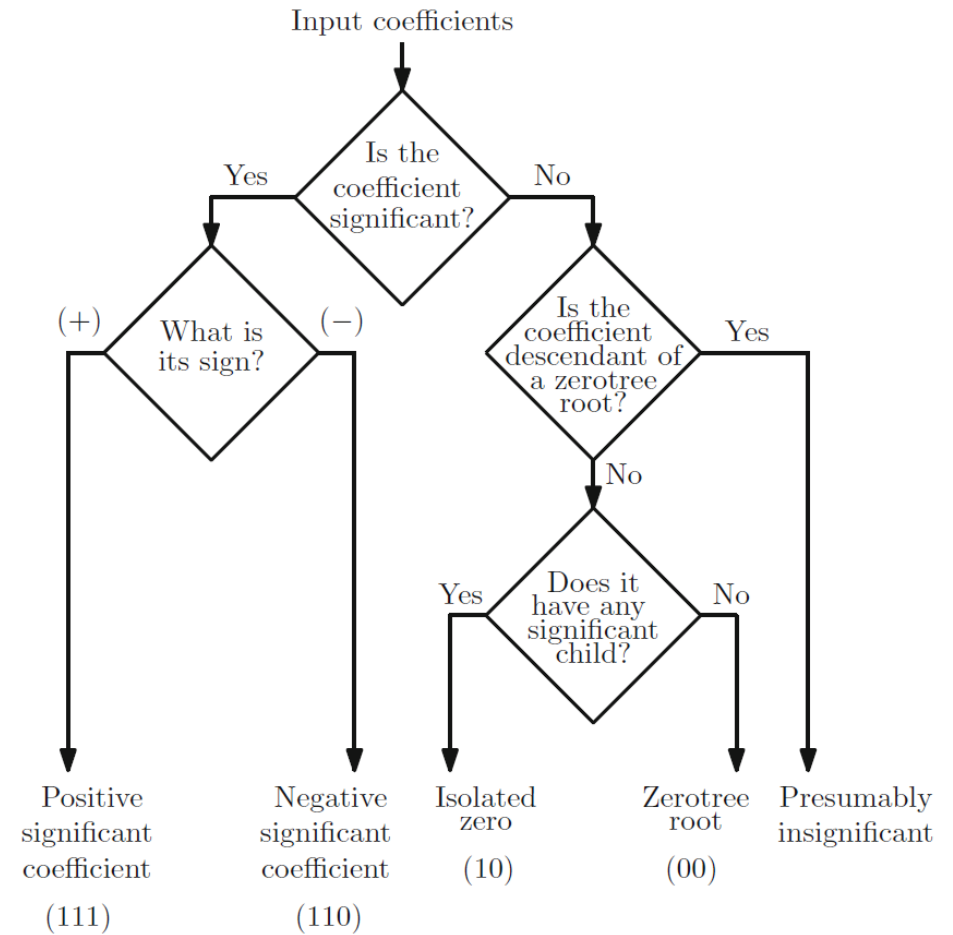
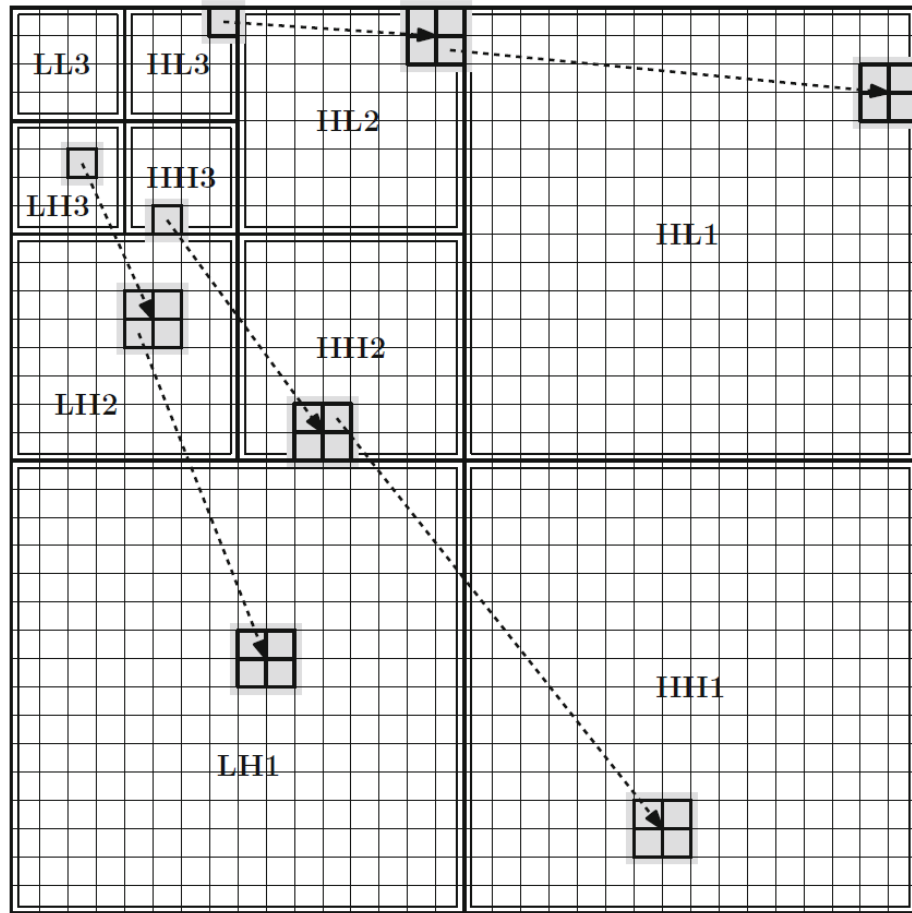
# PROPRIEDADES GLOBAIS DO CHIP

<b>Technology</b>	AMS CMOS 0.35 $\mu\text{m}$ Opto
<b>Chip Area</b>	1.61 mm $\times$ 1.28 mm
<b>Array Size</b>	32 $\times$ 32
<b>Block Area</b>	150 $\mu\text{m}$ $\times$ 150 $\mu\text{m}$
<b>Pixel Area</b>	37.5 $\mu\text{m}$ $\times$ 37.5 $\mu\text{m}$
<b>Photodiode Area</b>	10 $\mu\text{m}$ $\times$ 10 $\mu\text{m}$
<b>Fill Factor</b>	7%
<b>Power Supply</b>	3.3 V
<b>Power Consumption</b>	37 mW maximum (white image)
<b>Integration Period</b>	800 $\mu\text{s}$
<b>Conversion/Read-Out Time</b>	1 ms (one block-row)
<b>Achievable Frame Rate</b>	125 Hz
<b>FPN</b>	7%
<b>Temporal Noise</b>	4%
<b>Spatial Bandwidth</b>	2 cycles/cm
<b>Input Dynamic Range</b>	approx. 40 lux to 400 lux
<b>Data Rate</b>	below 0.94 bpp
<b>PSNR</b>	18 dB

# DECOMPOSIÇÃO SUB-BANDAS NO PLANO FOCAL

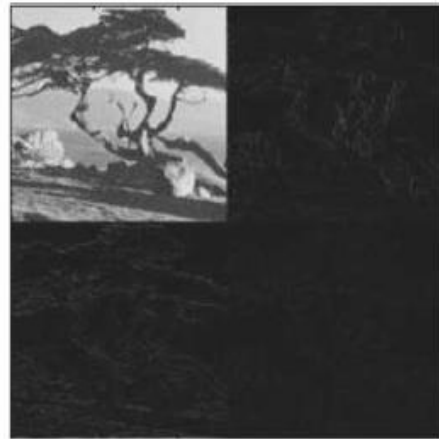


# DECOMPOSIÇÃO SUB-BANDAS NO PLANO FOCAL

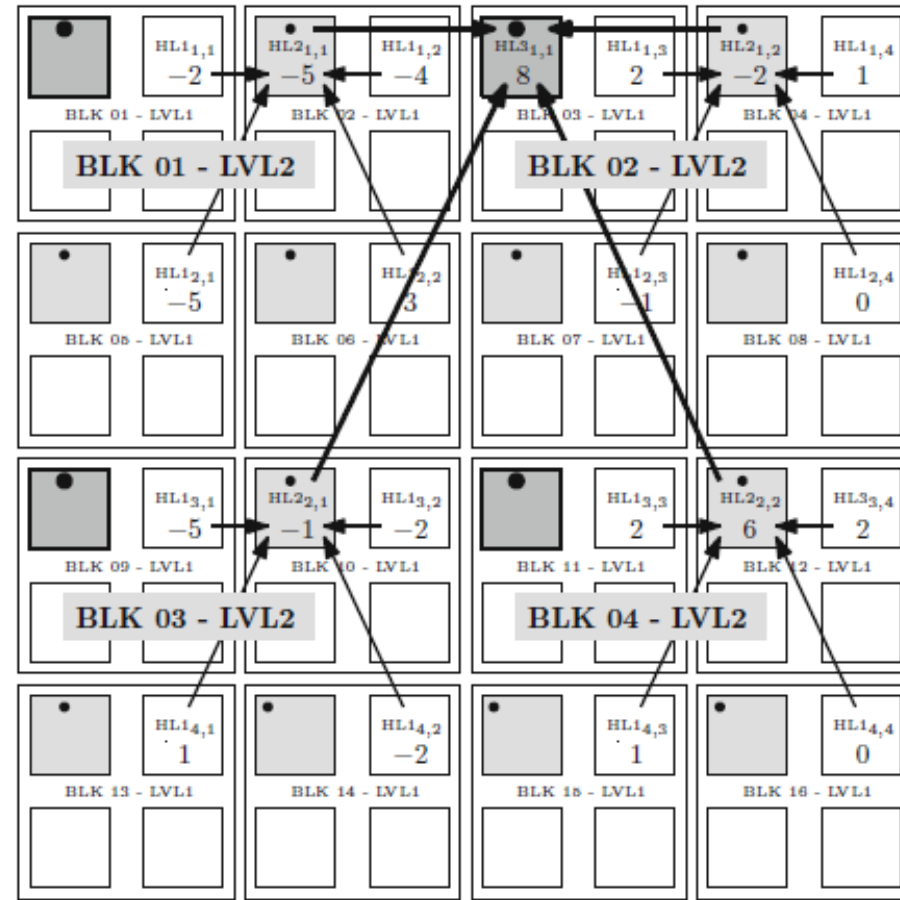




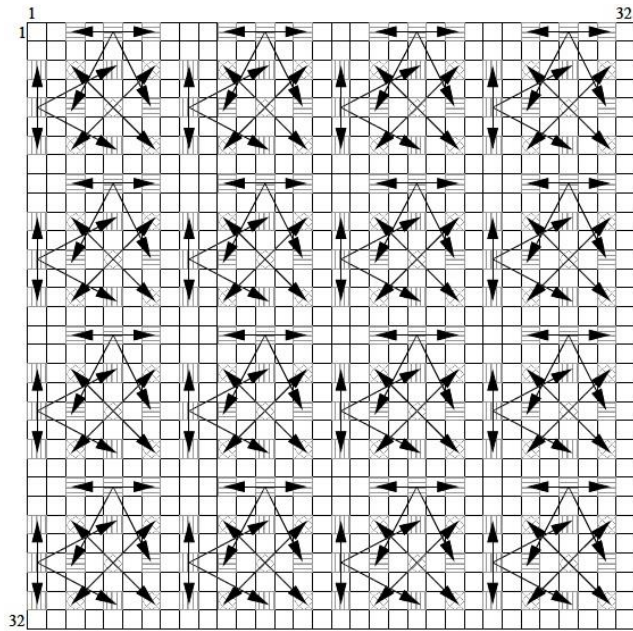
# DECOMPOSIÇÃO SUB-BANDAS NO PLANO FOCAL



LL2	HL2	HL1
LH2	HH2	
LH1		HH1



# DECOMPOSIÇÃO SUB-BANDAS NO PLANO FOCAL

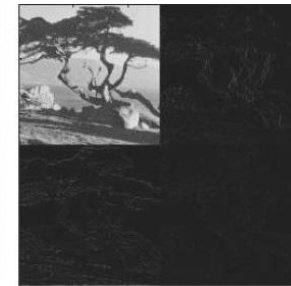


Legenda  
(sub-bandas):

-  HL
-  LH
-  HH



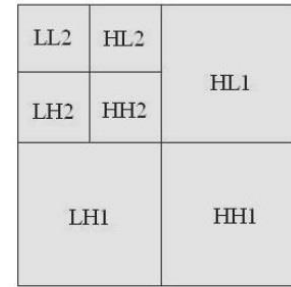
(a)



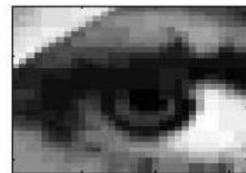
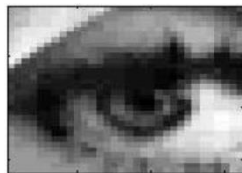
(b)



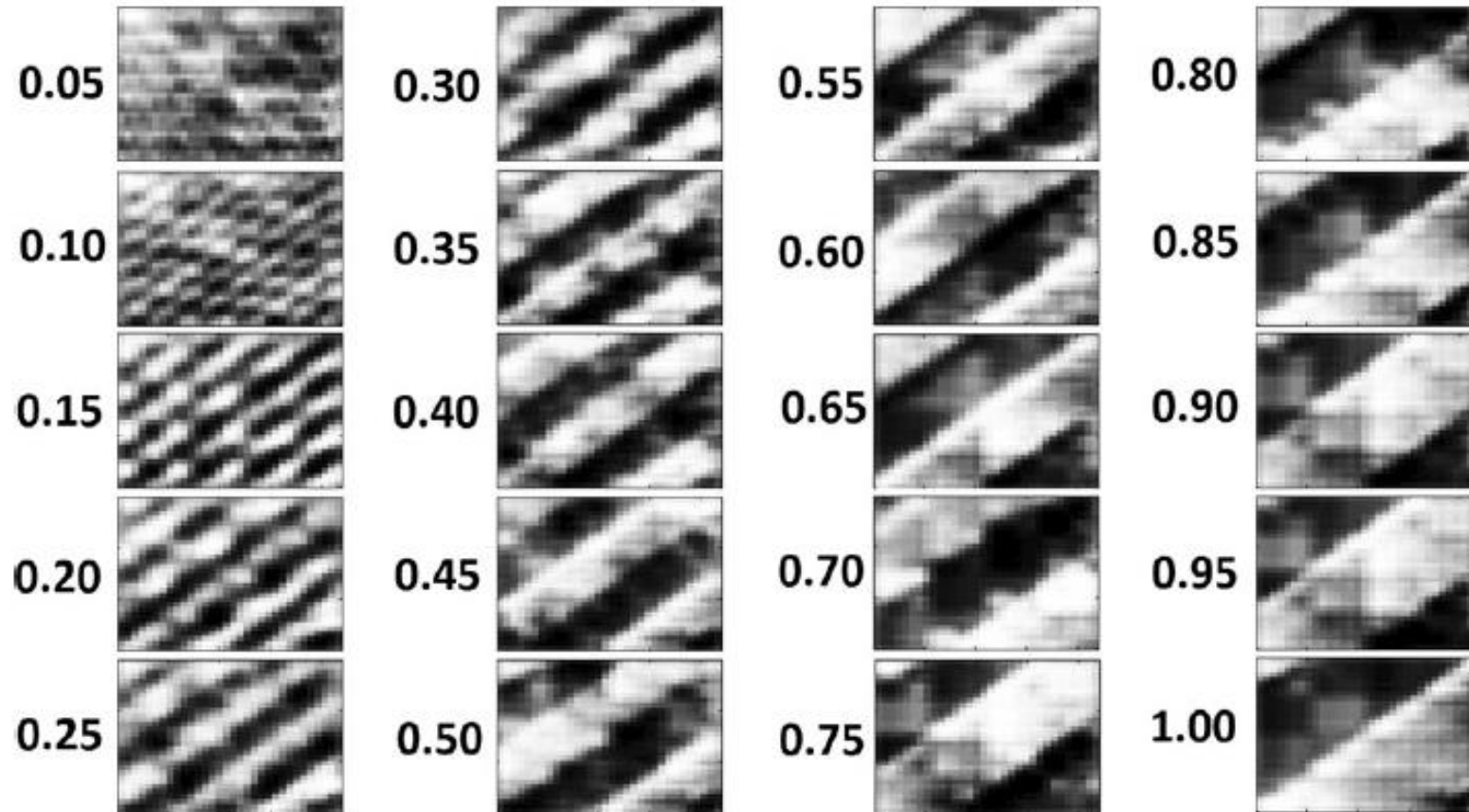
(c)



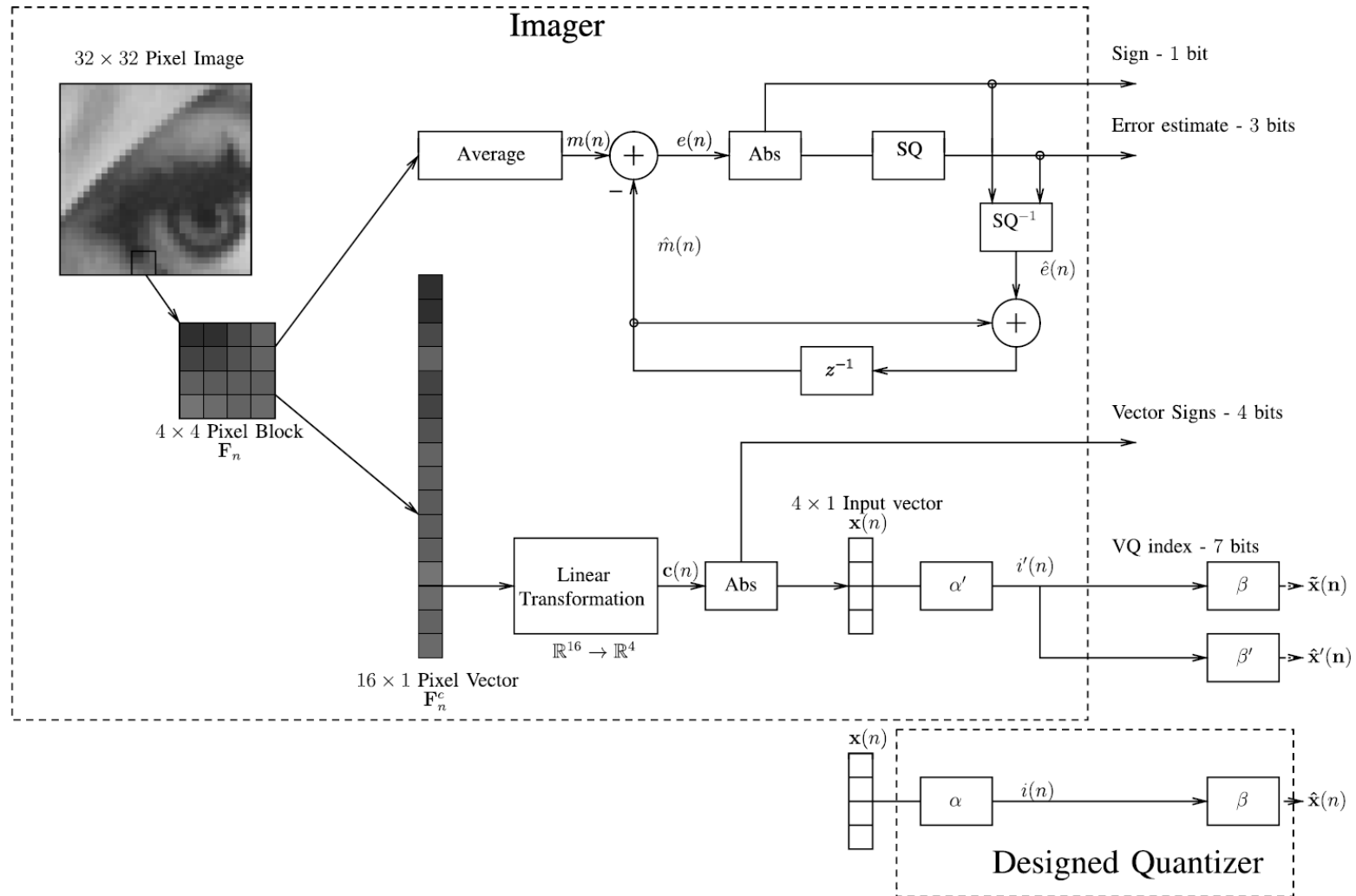
(d)



# DECOMPOSIÇÃO SUB-BANDAS NO PLANO FOCAL

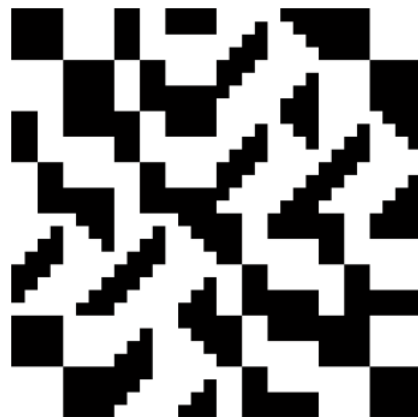


# CALIBRAÇÃO DE DICIONÁRIO

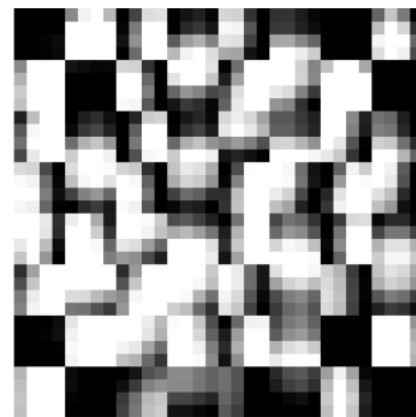


# CALIBRAÇÃO DE DICIONÁRIO

Target



Original



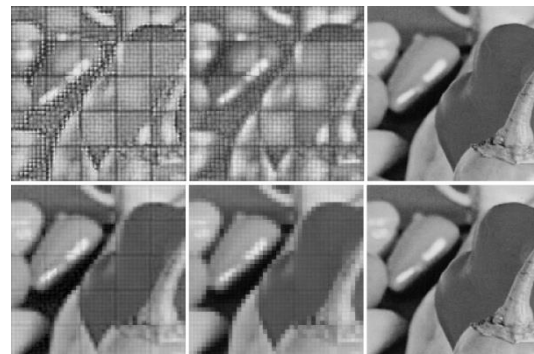
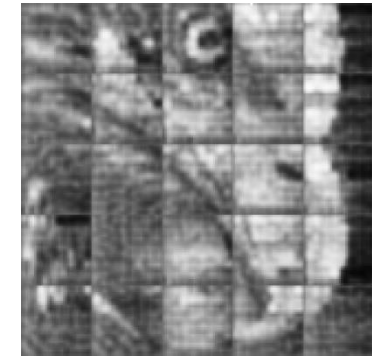
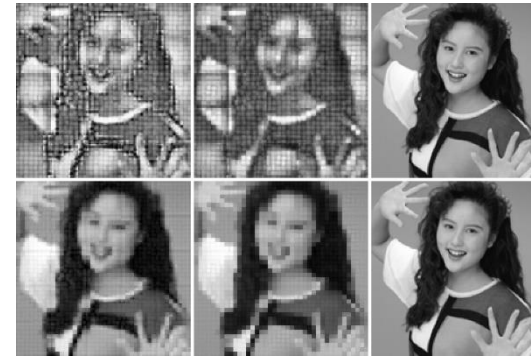
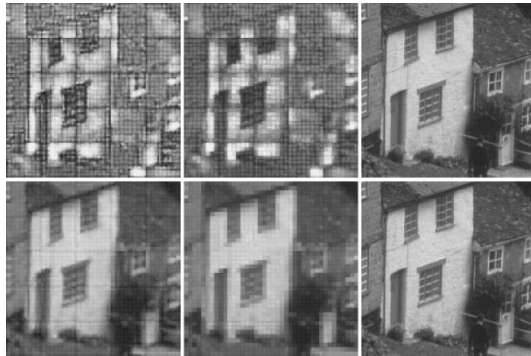
All



Specific



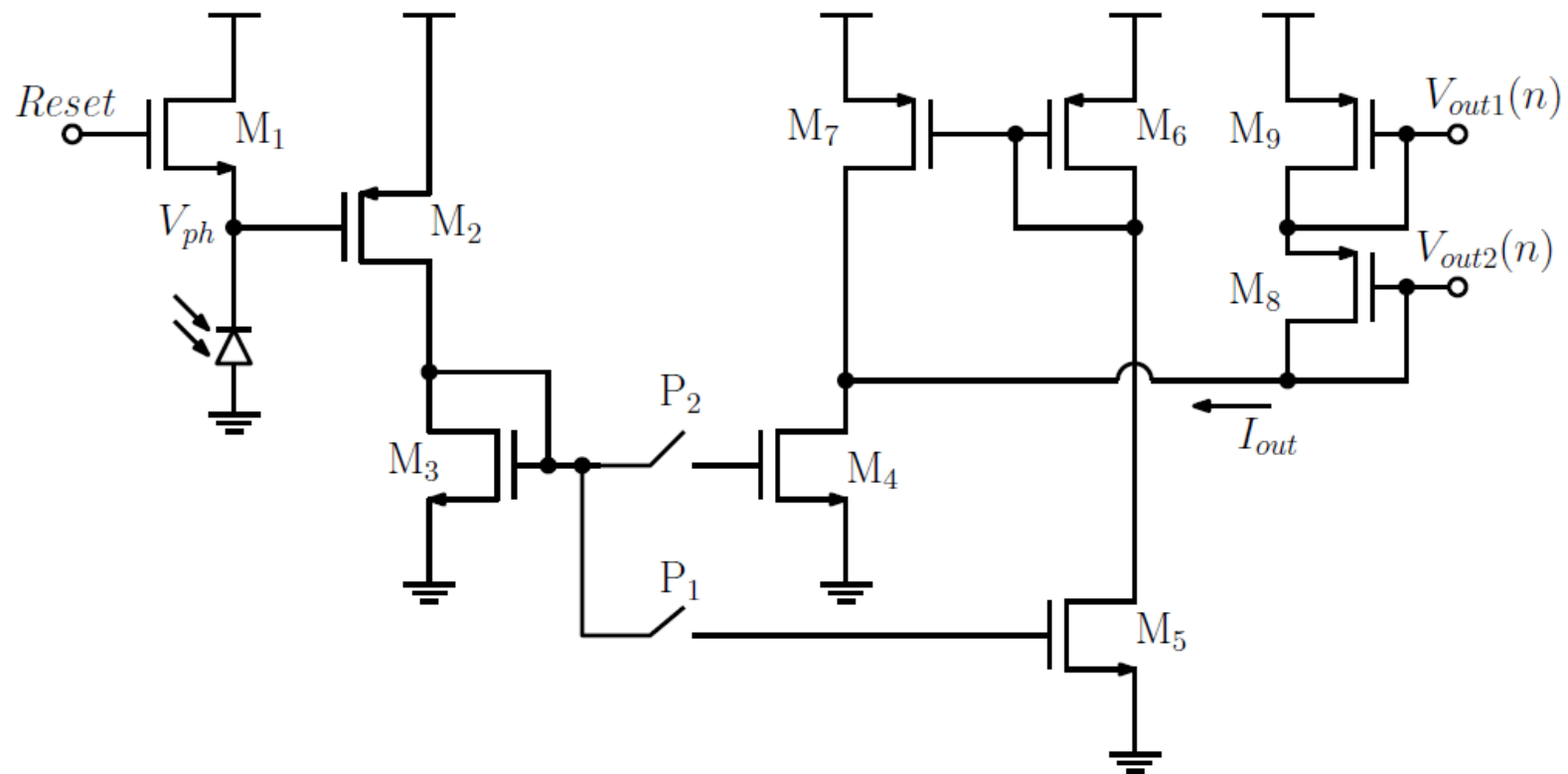
# CALIBRAÇÃO DE DICIONÁRIO



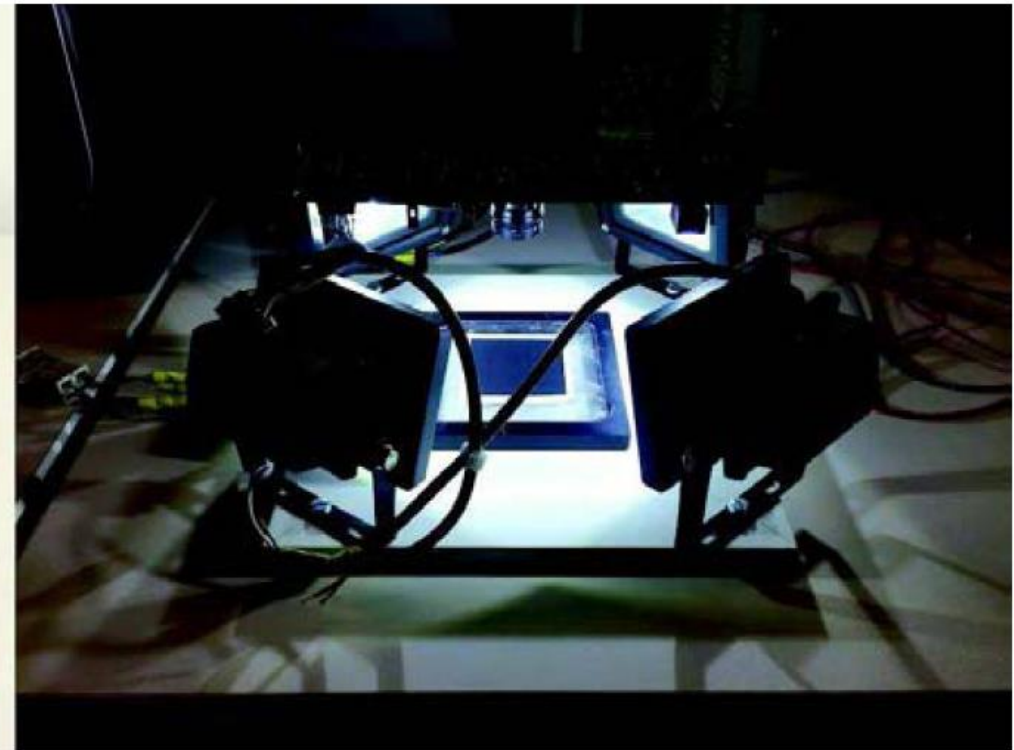
Decoded Image	Except	All	Original
Bike	0.0871	0.0852	0.0989
Bird	0.0503	0.0501	0.0632
Goldhill	0.0288	0.0284	0.0371
Lena	0.0303	0.0295	0.0392
Peppers	0.0235	0.0224	0.0269
Steve	0.0663	0.0659	0.0744
Vader	0.1049	0.1022	0.1073

# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL

- Diagrama de Blocos 0.18  $\mu\text{m}$ ; Cascode Current Mirror Pixels

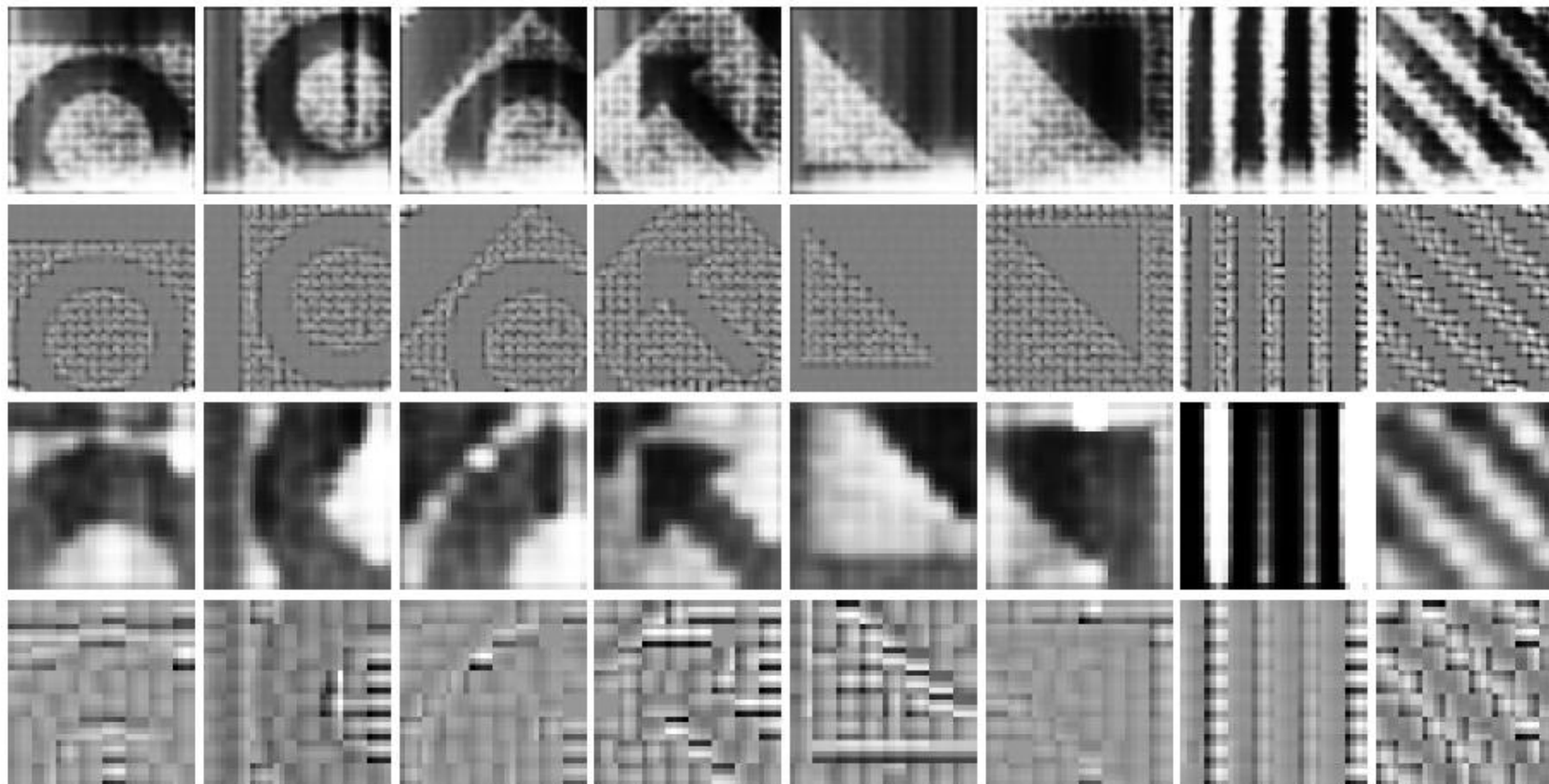


# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL





# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL

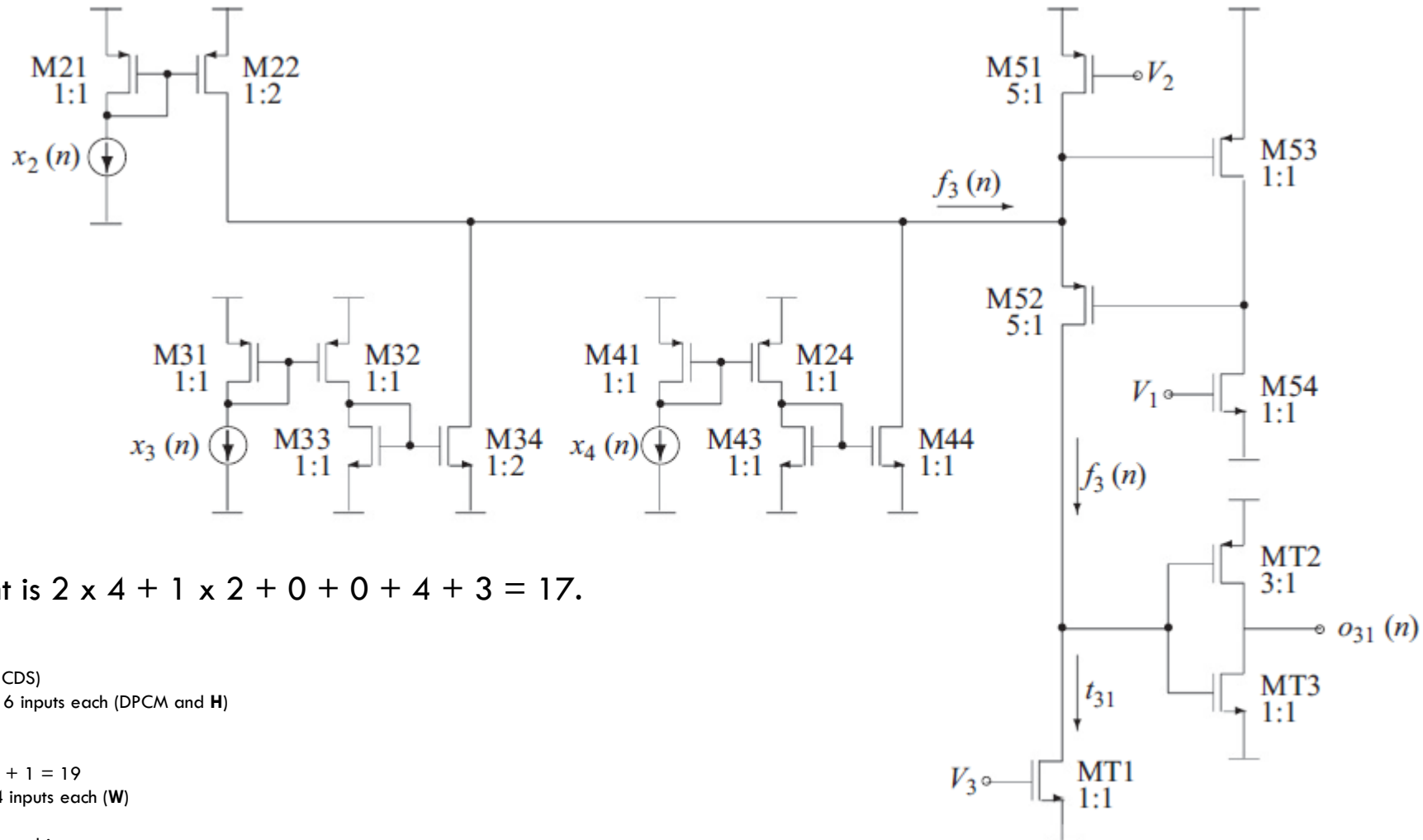


# CODIFICAÇÃO EM BLOCOS NO PLANO FOCAL

TABLE I  
COMPARISON BETWEEN FIRST AND SECOND GENERATION CHIPS.

	1 <sup>st</sup> generation	2 <sup>nd</sup> generation
Bit rate	0.94 bpp	1.13 bpp
Transform coeffs.	4	5
Sign bits	4	5
VQ bits	7	9
Fab. process	AMS 0.35 $\mu\text{m}$ Opto	IBM 0.18 $\mu\text{m}$
Transistor count	607 per block	833 per block
Pixel area	37.5 $\mu\text{m} \times 37.5 \mu\text{m}$	27.2 $\mu\text{m} \times 27.2 \mu\text{m}$
Photodiode area	10 $\mu\text{m} \times 10 \mu\text{m}$	10 $\mu\text{m} \times 10 \mu\text{m}$
Fill factor	7.1 %	13.5 %
Chip area	2.4 mm $\times$ 2.1 mm	2.8 mm $\times$ 2.8 mm
Resolution	32 $\times$ 32	64 $\times$ 64
DPCM $\hat{s}(1)$	0.0	7.5
Power supply	3.3 V	1.8 V

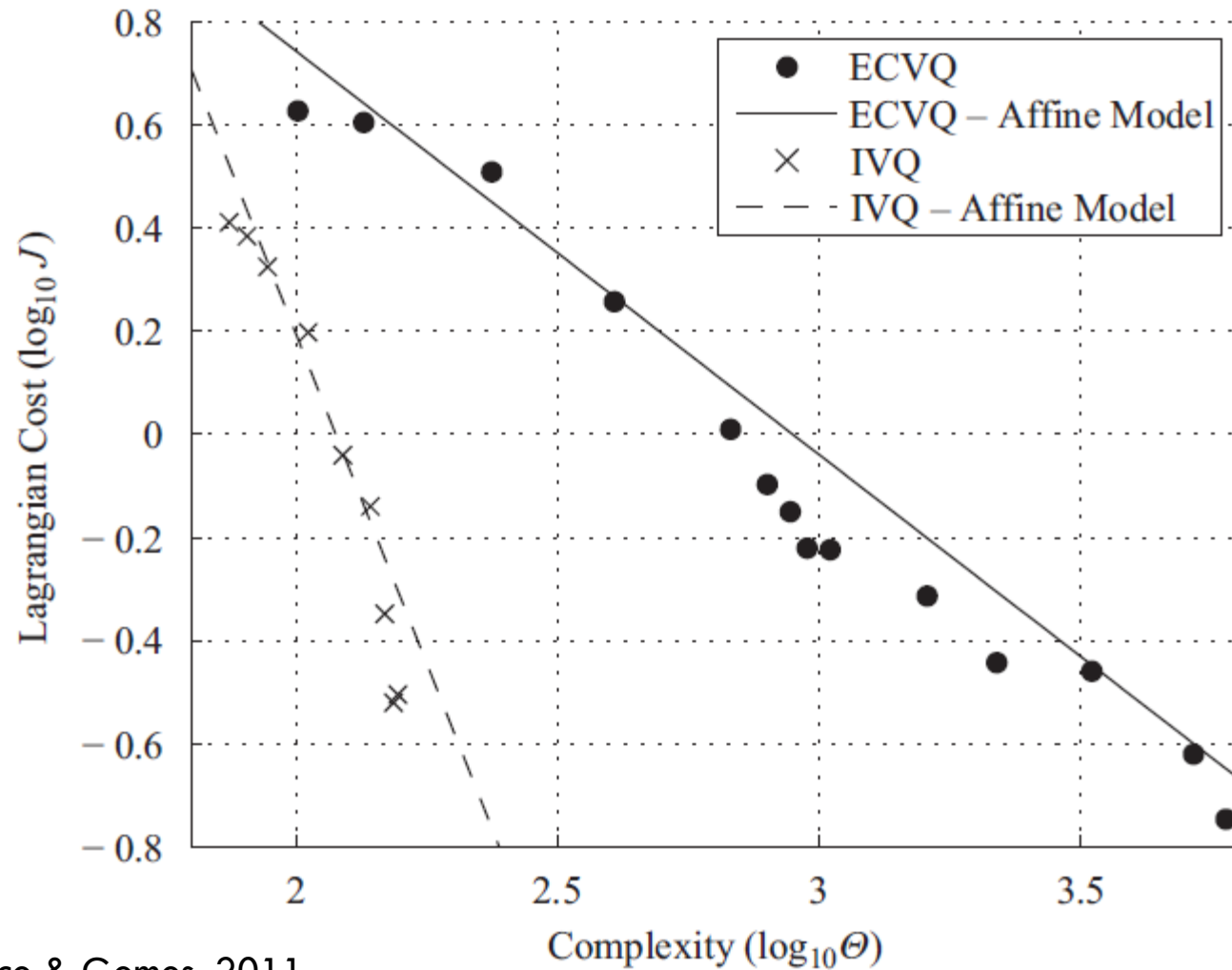
# ANÁLISE DE COMPLEXIDADE



- Transistor count is  $2 \times 4 + 1 \times 2 + 0 + 0 + 4 + 3 = 17$ .

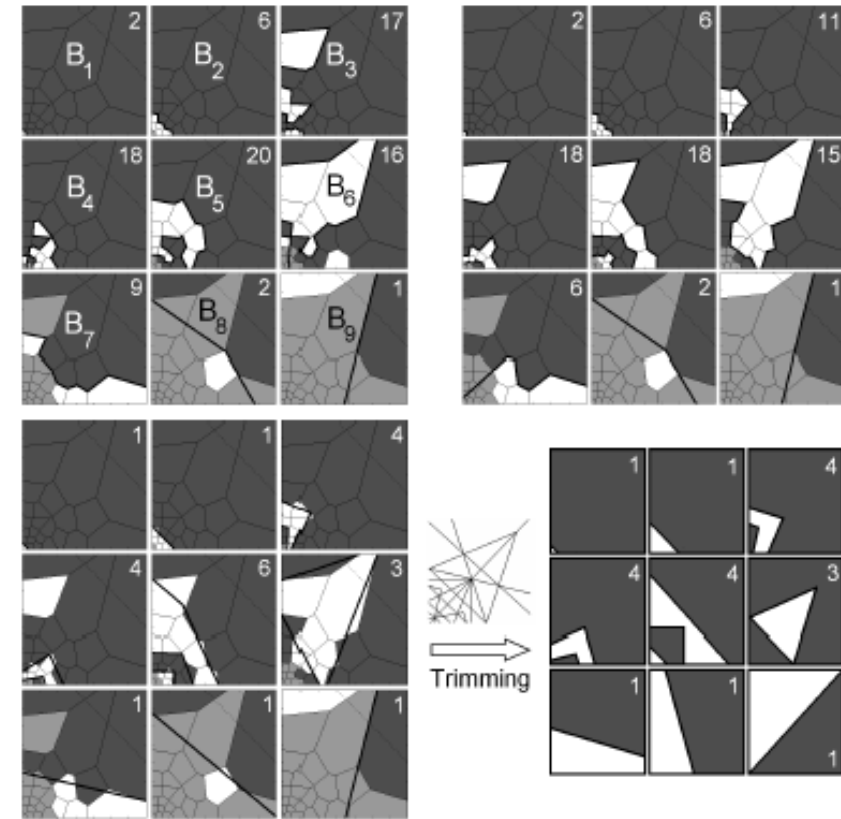
- 16 pixels (current mode with CDS)
- 5 inner-product circuits with 16 inputs each (DPCM and H)
- DPCM reconstruction circuit
- 5 absolute-value circuits
- Comparators:  $7 + 7 + 3 + 1 + 1 = 19$
- 4 inner-product circuits with 4 inputs each (W)
- 5 XNOR gates
- Row selection logic for 15 output bits

# ANÁLISE DE COMPLEXIDADE

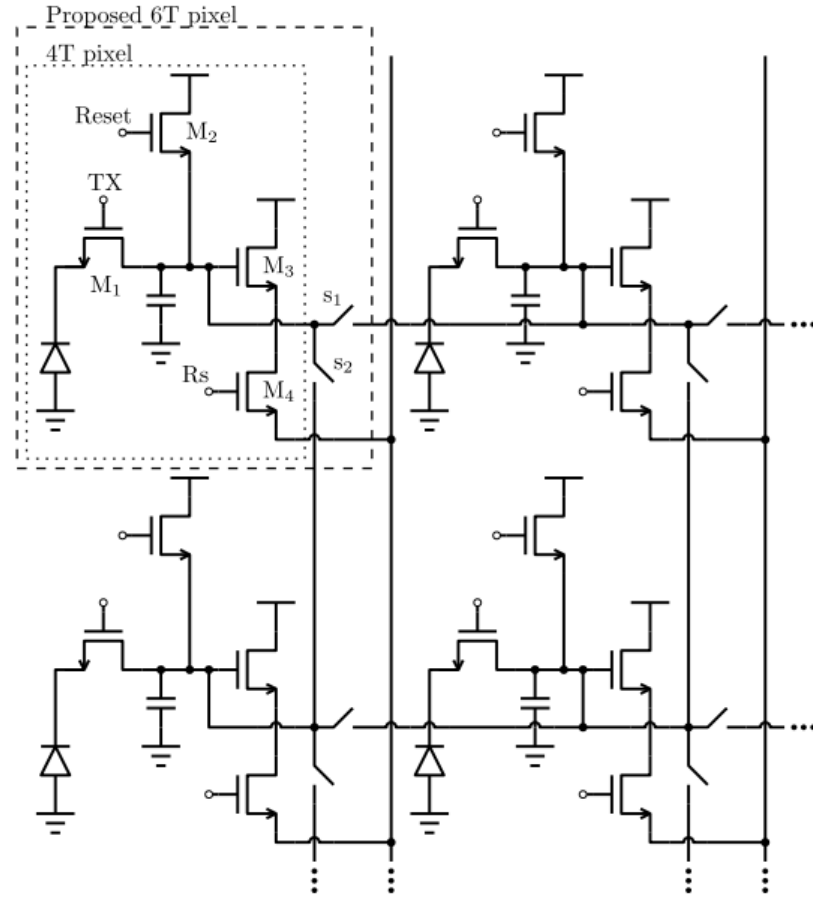


# ANÁLISE DE COMPLEXIDADE

	$B_1$	$B_2$	$B_3$	$B_4$	$B_5$	$B_6$	$B_7$	$B_8$	$B_9$	
01	0	x	x	x	x	x	x	x	x	1
02	1	0	0	x	x	x	x	x	x	3
03	1	0	1	0	x	x	x	x	x	4
04	1	0	1	1	1	x	x	x	x	5
05	1	1	0	0	1	x	x	x	x	5
06	1	0	1	1	0	x	x	x	x	5
07	1	1	0	0	0	x	x	x	x	5
08	1	1	1	0	0	1	x	x	x	6
09	1	1	0	1	0	0	x	x	x	6
10	1	1	1	0	1	1	x	x	x	6
11	1	1	0	1	1	1	x	x	x	6
12	1	1	0	1	1	0	x	x	x	6
13	1	1	1	0	1	0	x	x	x	6
14	1	1	0	1	0	1	x	x	x	6
15	1	1	1	0	0	0	x	x	x	6
16	1	1	1	1	0	1	0	x	x	7
17	1	1	1	1	0	1	1	x	x	7
18	1	1	1	1	0	0	1	x	x	7
19	1	1	1	1	0	0	0	x	x	7
20	1	1	1	1	1	0	0	x	x	7
21	1	1	1	1	1	1	0	x	x	7
22	1	1	1	1	1	0	1	x	x	7
23	1	1	1	1	1	1	1	0	x	8
24	1	1	1	1	1	1	1	1	1	9
25	1	1	1	1	1	1	1	1	0	9



# GAUSSIAN PYRAMID TIME/ENERGY ANALYSIS



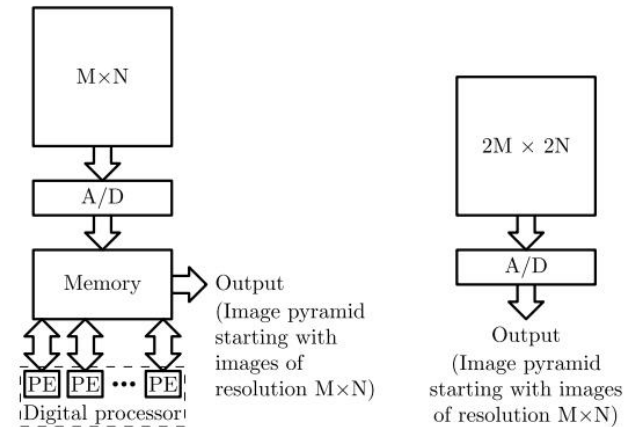
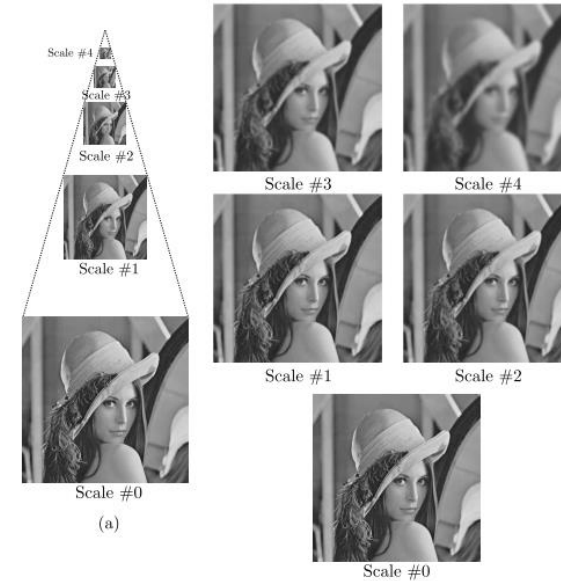
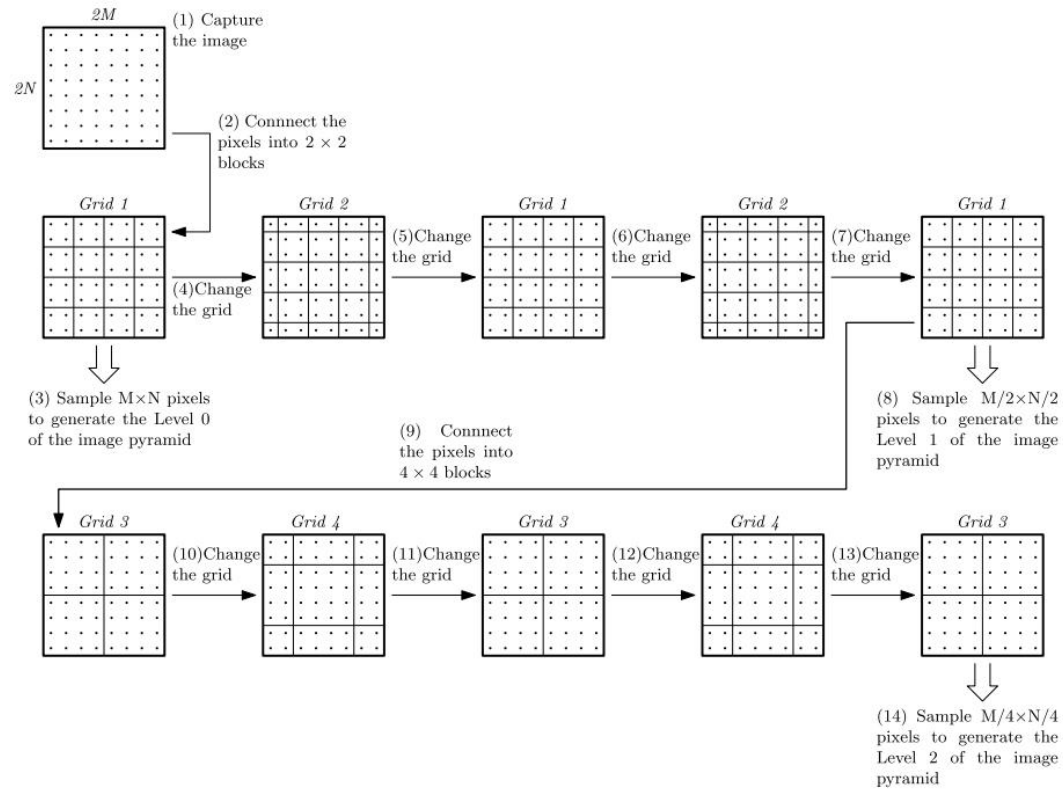
2	1	20	0	0	0	1	2
7	6	13	15	14	34	6	7
9	3	40	20	23	13	44	5
0	4	16	100	11	1	80	15
10	12	30	104	14	1	50	31
18	8	3	7	1	0	17	14
20	107	71	11	12	10	60	19
7	10	21	9	2	24	1	0

4 4 <i>p<sub>i-1,j-1</sub></i>	12 12 <i>p<sub>i-1,j</sub></i>	12 12 <i>p<sub>i-1,j+1</sub></i>	4 4 <i>p<sub>i-1,j+2</sub></i>
4 4	12 12	12 12	4 4
4 4 <i>p<sub>i,j-1</sub></i>	44 44 <i>p<sub>i,j</sub></i>	12 12 <i>p<sub>i,j+1</sub></i>	36 36 <i>p<sub>i,j+2</sub></i>
4 4	44 44	12 12	36 36
12 12 <i>p<sub>i+1,j-1</sub></i>	36 36 <i>p<sub>i+1,j</sub></i>	4 4 <i>p<sub>i+1,j+1</sub></i>	28 28 <i>p<sub>i+1,j+2</sub></i>
12 12	36 36	4 4	28 28
36 36 <i>p<sub>i+2,j-1</sub></i>	28 28 <i>p<sub>i+2,j</sub></i>	12 12 <i>p<sub>i+2,j+1</sub></i>	20 20 <i>p<sub>i+2,j+2</sub></i>
36 36	28 28	12 12	20 20

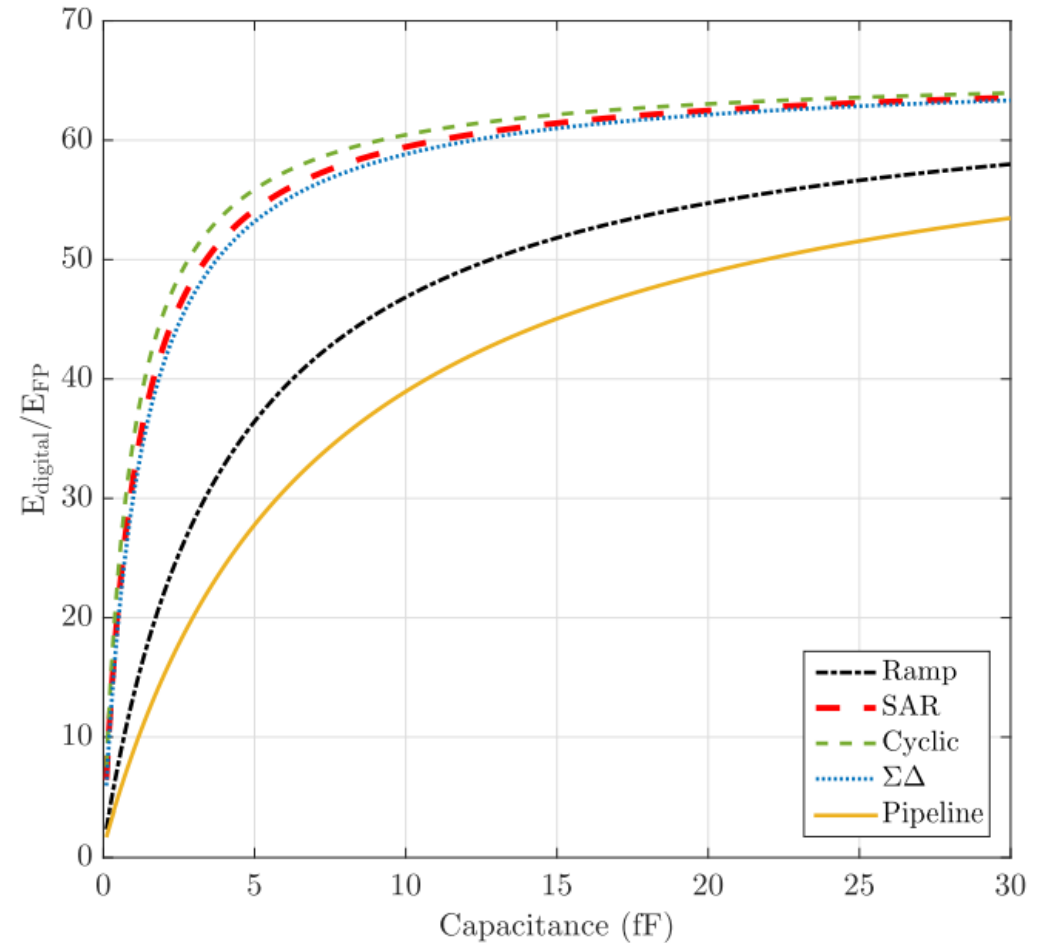
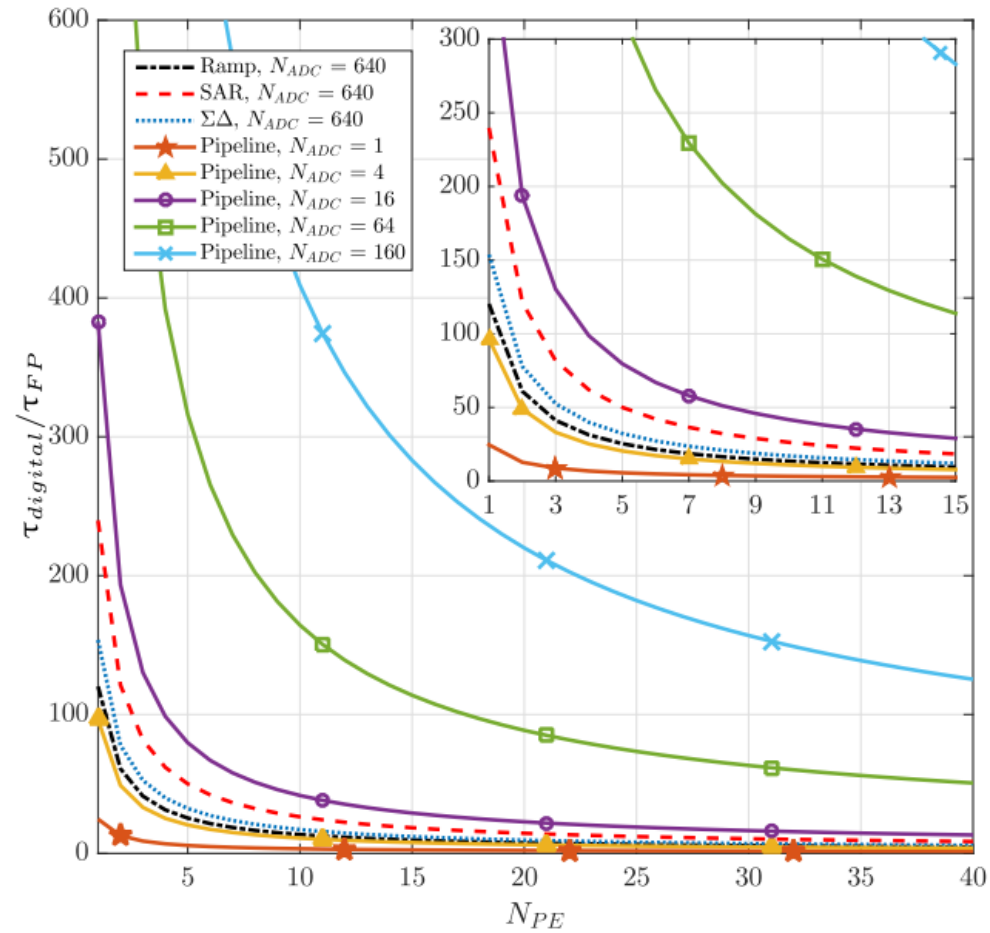
4	8	8	12	12	8	8	4
4	16	16	20	20	16	16	20
4	16	16	20	20	16	16	20
8	24	24	24	24	20	20	32
8	24	24	24	24	20	20	32
24	28	28	20	20	16	16	24
24	28	28	20	20	16	16	24
36	32	32	20	20	16	16	20

8	8	14	14	14	14	12	12
8	8	14	14	14	14	12	12
13	13	21	21	20	20	22	22
13	13	21	21	20	20	22	22
21	21	24	24	20	20	23	23
21	21	24	24	20	20	23	23
30	30	25	25	18	18	19	19
30	30	25	25	18	18	19	19

# GAUSSIAN PYRAMID TIME/ENERGY ANALYSIS

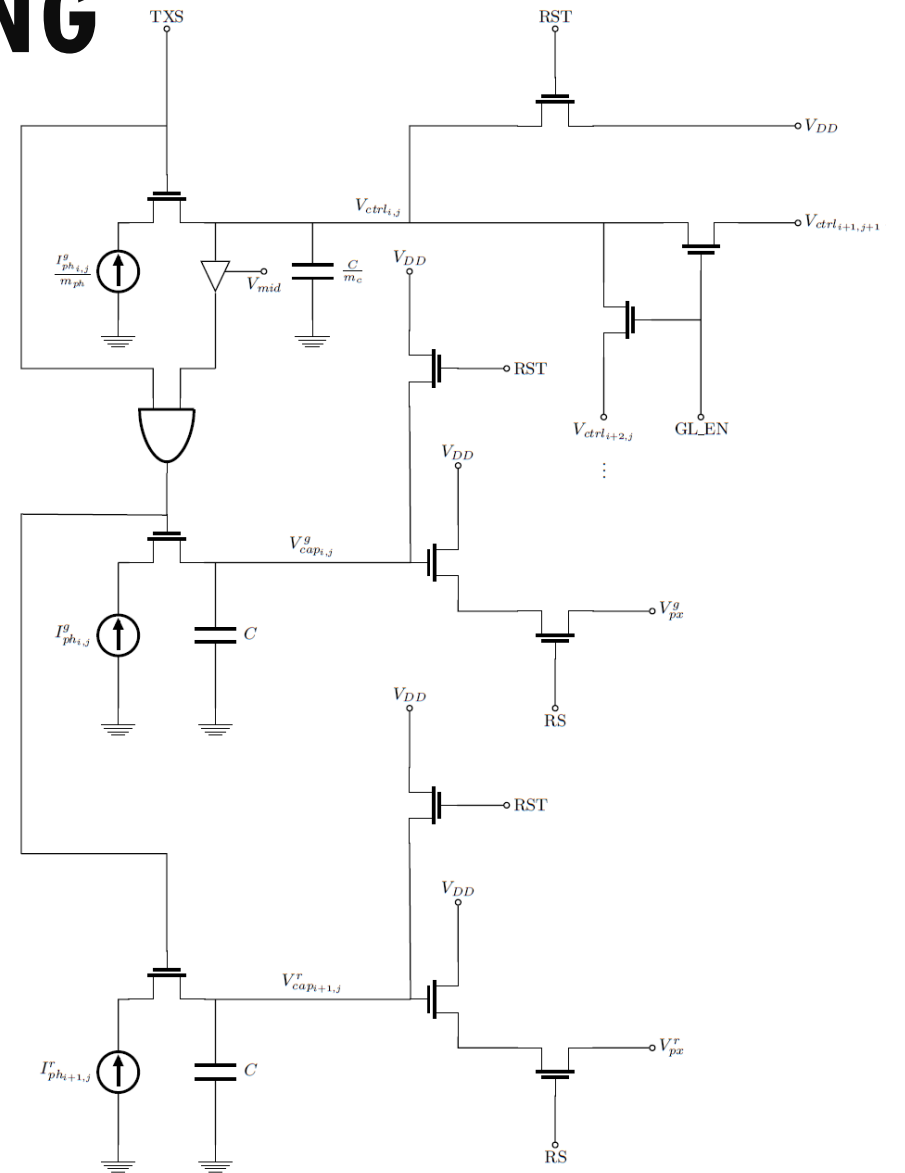
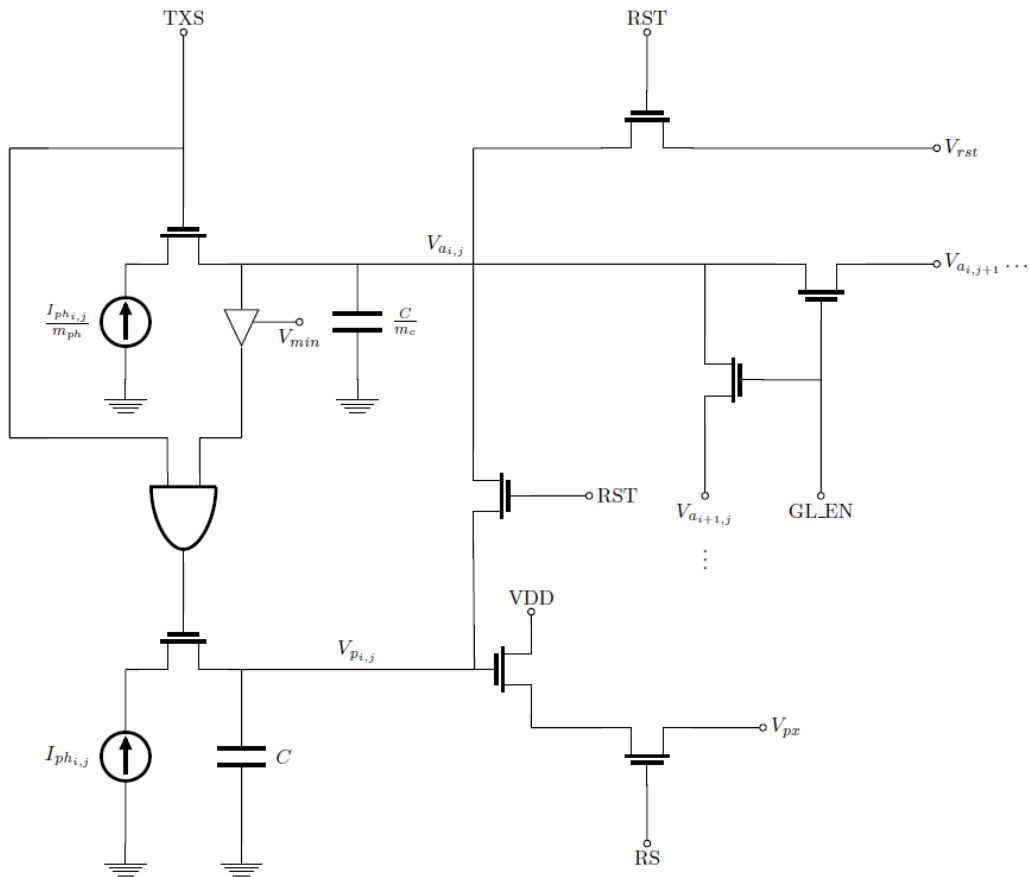


# GAUSSIAN PYRAMID TIME/ENERGY ANALYSIS

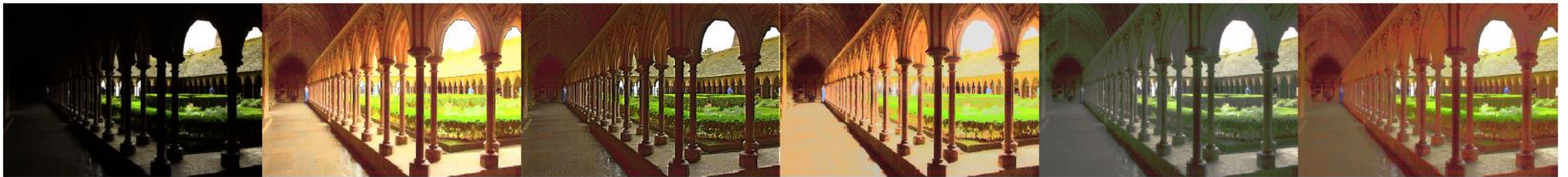




# HIGH DYNAMIC RANGE IMAGING



# HIGH DYNAMIC RANGE IMAGING



**Raw**

**Schlick**

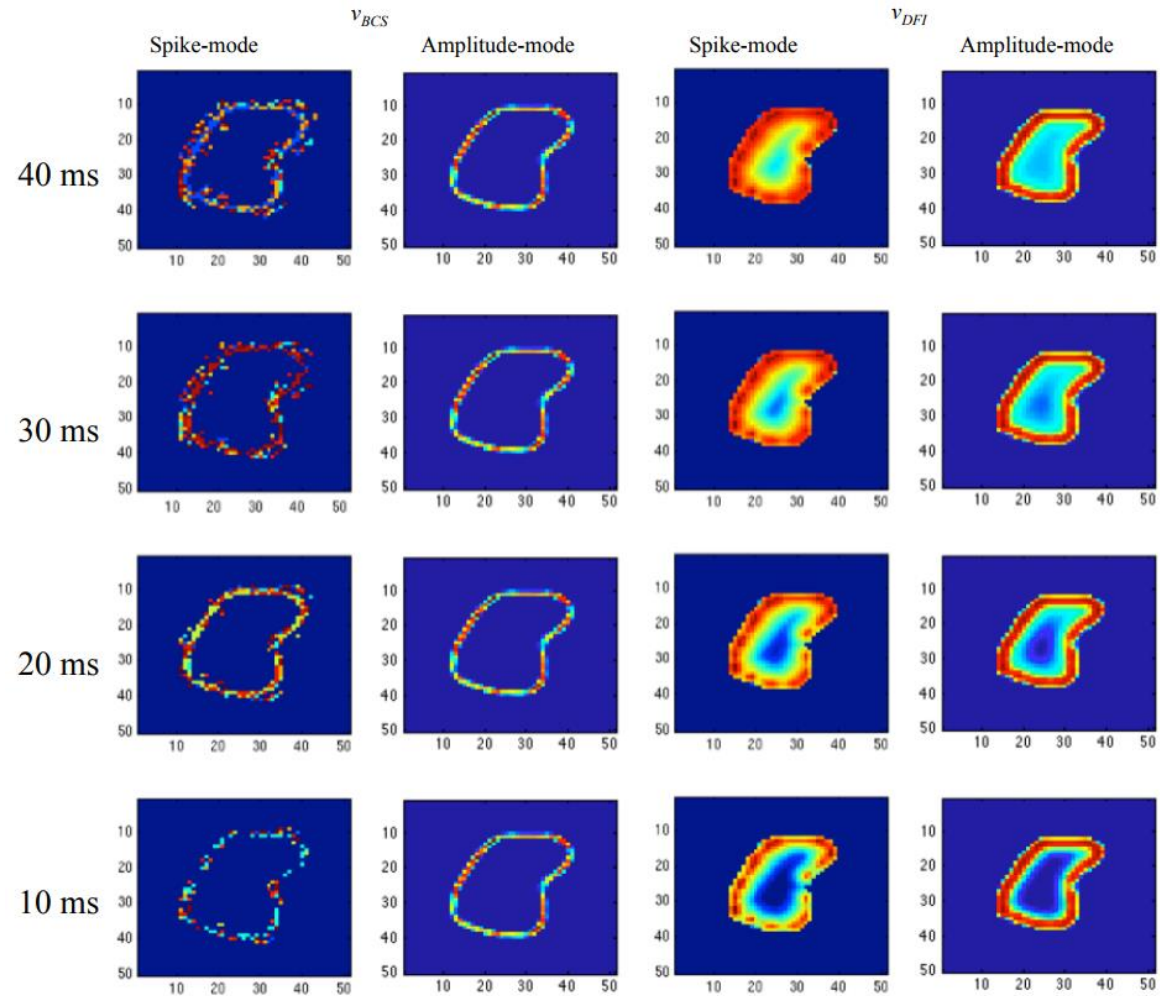
**Rahman**

**WB + Y TM**

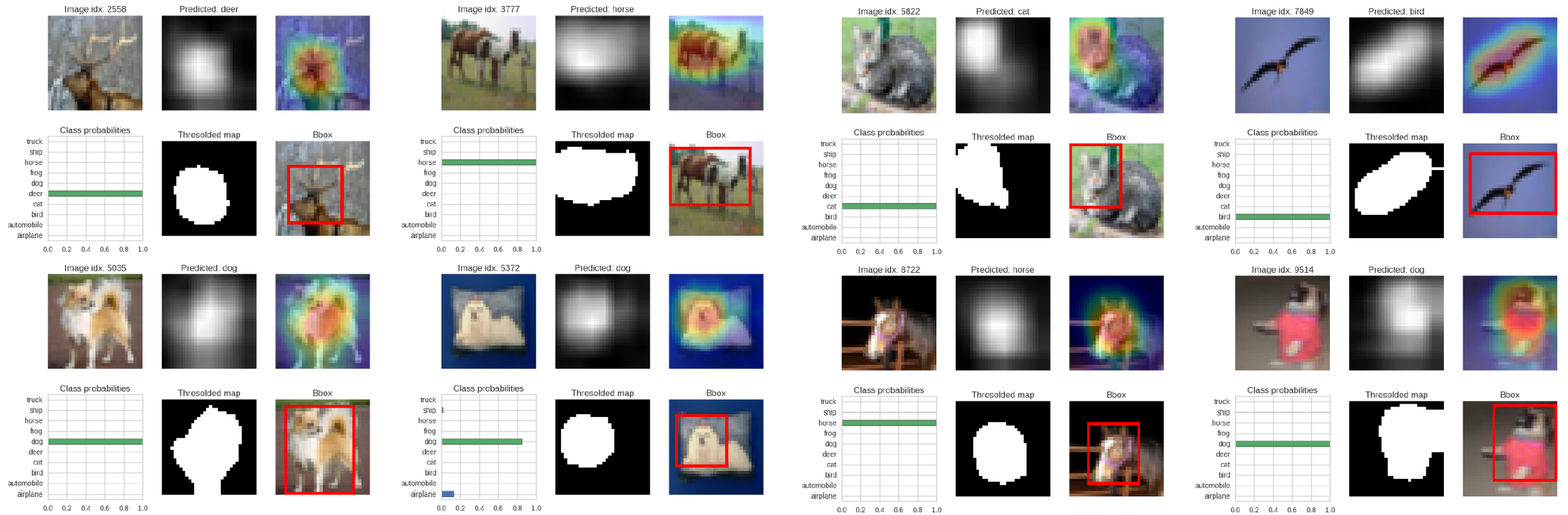
**F. Plane RGB**

**F. Plane Green**

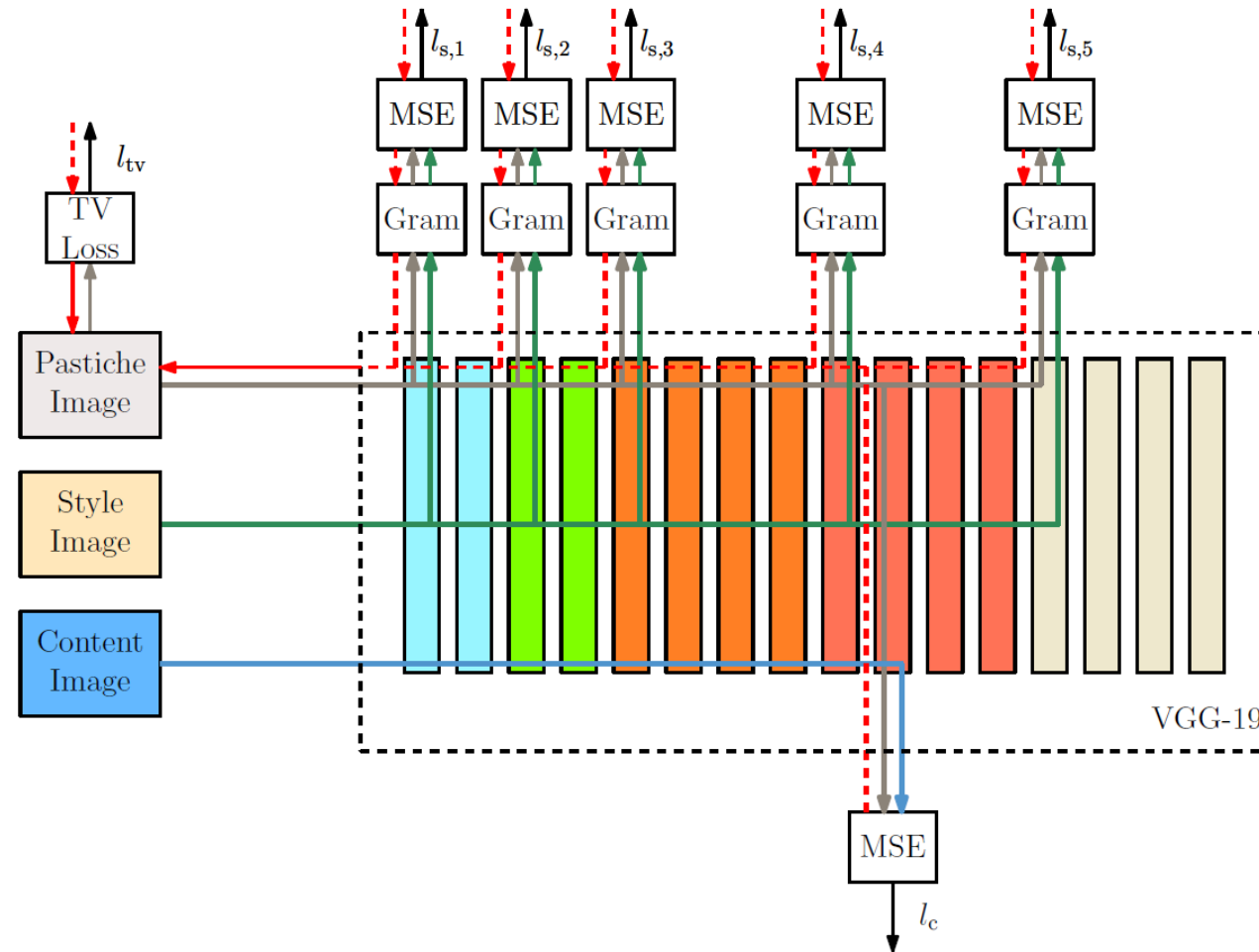
# DIFFUSIVE FILLING-IN



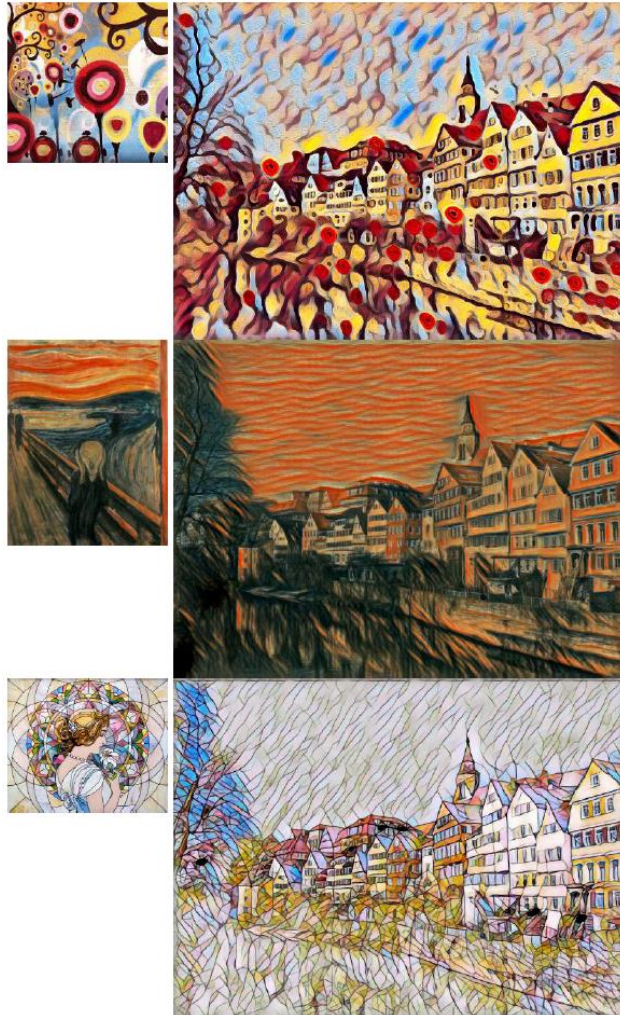
# DEEP LEARNING – CLASS ACTIVATION MAPS



# DEEP LEARNING – NEURAL STYLE TRANSFER



# DEEP LEARNING – NEURAL STYLE TRANSFER



# OUTRAS IDÉIAS

- **Compressão de imagens no plano focal aparece em diversas outras referências. Uma tabela comparativa é dada em [Oliveira, 2013].**
- **Há também filtragem (convoluções), detecção de bordas, estimação de movimento, visão estéreo, reconhecimento de padrões.**
- **Abordagens (menos ou mais recentes) à visão computacional utilizando sinais pulsados.**

# TENDÊNCIAS PARA O FUTURO

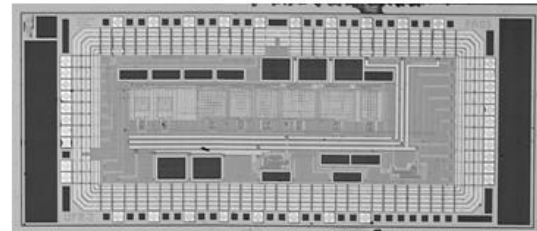
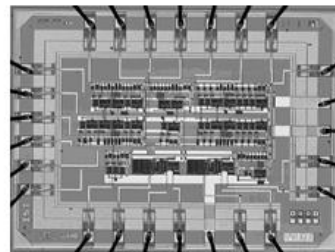
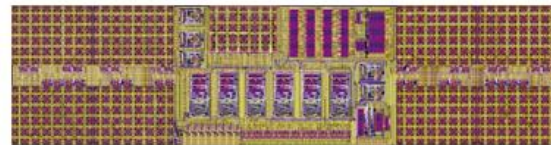
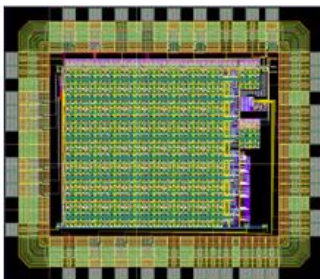
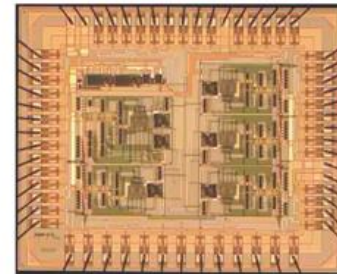
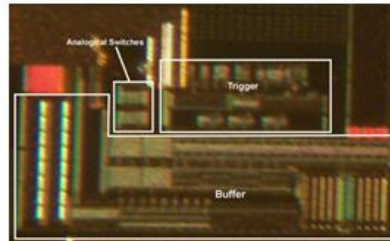
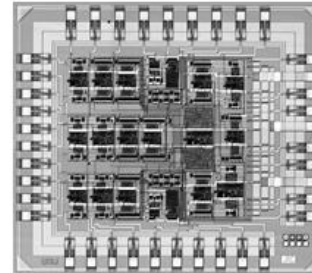
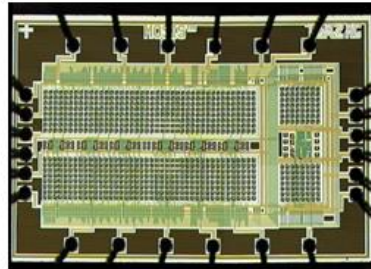
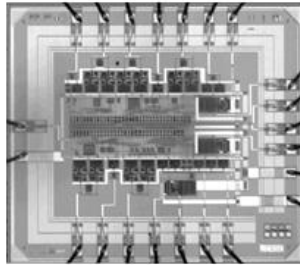
- **High dynamic range imaging**
- **Compressive sensing**
- **Z. Chen, A Primer on Neural Signal Processing, IEEE CAS Magazine, First Quarter 2017**
- **M. Ahmed and B. K. Sujatha, A review on methods, issues and challenges in neuromorphic engineering, em Anais IEEE ICCSP 2015**
- **A. Yousefzadeh, T. Masquelier, T. Serrano-Gotarredona, and B. Linares-Barranco, Hardware implementation of convolutional STDP for on-line visual feature learning, em Anais ISCAS 2017**
- **S. Walz, J. Miller and R. Tetzlaff, Image classification by cellular nonlinear networks, em Anais ISCAS 2017**



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- R. M. Estevão Filho, A Study on Deep Convolutional Neural Networks for Computer Vision Applications, Dissertação de Mestrado, PEE/COPPE/UFRJ, 2017.

# AGRADECIMENTOS



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CNPq

CAPES

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Joarez B. Monteiro

Alunos do PADS/COPPE/UFRJ



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